MSC8144AMC-S Advanced Mezzanine Card User Manual

MSC8144AMCSUM
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Chapter 1
General Information

1.1 Introduction

This document describes the MSC8144AMC-S AdvancedMC (AMC) Card. The MSC8144AMC-S provides an AMC debugging environment for engineers developing applications for the MSC8144 series of Freescale Processors.

The MSC8144 is a highly integrated DSP processor that contains four StarCore® SC3400 DSP subsystems, 512 Kbytes of M2 shared memory, 10 Mbytes of M3 shared memory, L1 instruction and data caches, 128 Kbytes of shared L2 instruction cache, a DDR memory controller, a serial RapidIO® interface, two 10/100/1000Base-T Ethernet Controllers, an ATM Controller Supporting various ATM adaptation layers, eight 512-channel time division multiplexing (TDM) interfaces, a 16-channel DMA Controller, 32-bit PCI interfaces, UART interface and an I^2C interface.

The MSC8144AMC-S single-width AMC board is designed around four Freescale MSC8144s. Each MSC8144 has 256 Mbytes of associated 32-bit-wide DDR2. High throughput serial RapidIO links connect the four MSC8144s to each other and to the data backplane. The serial RapidIO interfaces can run in x1 or x4 mode and are interconnected via a TSI578 serial RapidIO switch. For the control plane, each MSC8144 RGMII Gigabyte Ethernet port is linked to the backplane ports via an Ethernet switch.

The 32 TDM lines (16 Rx and 16 Tx) are routed to the backplane from each MSC8144. All TDM Modules, with two links per module, are connected together over a common bus to achieve the 32 TDM line requirements. This TDM linkage to the backplane is optional and can be isolated when not required.

For bootstrap purposes, a common serial I^2C bus and EEPROMs are connected between the MSC8144s. The EEPROM is programmed through a master MSC8144 or an in-circuit programmer attached to a header.

AMC board management is handled via a CorEdge enabled Module Management Controller based around a Freescale MCF5213. The provides the board with power sequencing, hot swap functionality, temperature sensing and FRU record storage.

Due to space restrictions on the PCB, a number of debug and programming headers are offloaded to an expansion card via the front panel.

1.2 Working Configurations

There are two configurations for use of the MSC8144AMC-S board: system development environment or standalone.

1.2.1 System Development Environment

Freescale recommends that the AMC be run using an ATCA, µTCA, picoTCA chassis, or equivalent. This delivers the correct power and air flow to the board. I nsert the board into the carrier chassis as defined by the specific carrier instructions. As in standard development systems, these chassis provide direct connections to the JTAG debugger and external connections.

1.2.2 Standalone Operation

An external keyed power supply connector is provided for standalone operation. When using a standalone board, you must ensure that adequate cooling is provided for the board. Remove the front panel to access the connector.

1.3 MSC8144AMC-S Processor Board

The following subsystems provide a detailed description of the board and its connectors.

1.3.1 MSC8144AMC-S Features

- Target use
  - — System component for baseband, media gateway, and RNC systems
  - — Software development platform for baseband, media gateway, and RNC solutions
  - — Design reference and enablement platform for customers and third parties
- Form factor. Single-width AMC size, full height Module
- Connectivity
  - — Two serial RapidIO x4 interfaces from backplane ports 4–7 and 8–11 routed to DSP farm via a serial RapidIO switch
  - — 1000 Base-X Gigabit Ethernet from backplane ports 0 and 1 routed to DSP farm via Ethernet switch
  - — Gigabit Ethernet routed to front plane expansion connector via a switch
  - — E1/T1 TDM connection consisting of 8x (TX + RX) and common clock and sync on an AMC connector
  - — Each MSC8144 UART interface is multiplexed via the CPLD to a single RS-232 connector on the expansion connector
  - — I^2C Bus connecting MSC8144s for boot and configuration

- Hardware Blocks
  - Four MSC8144 DSPs (four cores per device), each with the following:
    - x4 serial RapidIO interface routed to a serial RapidIO switch
    - RGMII interface routed to an Ethernet switch
    - TDM routed to a CPLD for multiplexing to the backplane
    - I^2C interface for boot
    - 256 Mbytes of 32-bit DDR2 memory
  - Tundra TSI578 serial RapidIO switch
    - 4 lanes of x4 serial RapidIO lines from the MSC8144 farm
    - 2 lanes of x4 serial RapidIO lines to ports 4–7 and 8–11 of the backplane
    - 2 lanes of x4 serial RapidIO lines to ports 12–15 and 17–20 of the backplane
    - Controlled via I^2C or master MSC8144
  - Ethernet switch
    - 4 lanes of RGMII from the MSC8144 farm
    - 2 lanes of 1000Base-X to ports 0 and 1 of the backplane
    - 1 lane of SGMII to the front panel expansion connector
  - TDM. MSC8144 TDM routed to backplanes ports 12–15 and 17–20 (multiplexed with the serial RapidIO lines)
  - UART. MSC8144 UARTs multiplexed to the expansion connector
- Boot. Boot mode defined by switch:
  - Serial RapidIO interface via the backplane
  - From the on-board I^2C
- MSC8144 Debug. Chained JTAG header for four MSC8144s
- Board Management
  - Hot Swapping
  - FRU Storage
  - Status LEDs
  - Temperature and voltage monitoring
- Power Supply
  - 12 V and 3.3 V IPMCV, provided from AMC edge connector or terminal connector
  - On board voltage requirements are generated via DC-DC voltage regulators:
    - 3.3 V for I/O
    - 1.0 V for the MSC8144 cores and PLLs
    - 2.5 V for M3 memory
    - 1.25 V for MSC8144 M3 memories and the TSI578 core
    - 1.8 V/0.9 V DDR2
    - 1.2 V, 1.5 V, and 2.5 V for the Ethernet switches

1.3.2 External Connectors

The MSC8144AMC-S interconnects with external devices via the following set of connectors (see Figure 1-1 and Figure 1-2):

- AMC connector for connecting to ATCA and µTCA backplanes (P1)
- MSC8144 OnCE 14-pin Debug connector (HD2)
- CPLD programming header, 10 pin (HD1)
- Standalone power connector (P2)
- Expansion connector (J1) giving access to the following:
  - MSC8144 UART
  - Front panel Ethernet RJ45
  - Ethernet Switch EEPROM programming header
  - ColdFire® (MMC) BDM
  - ColdFire (MMC)UART
  - External I^2C EEPROM programming header

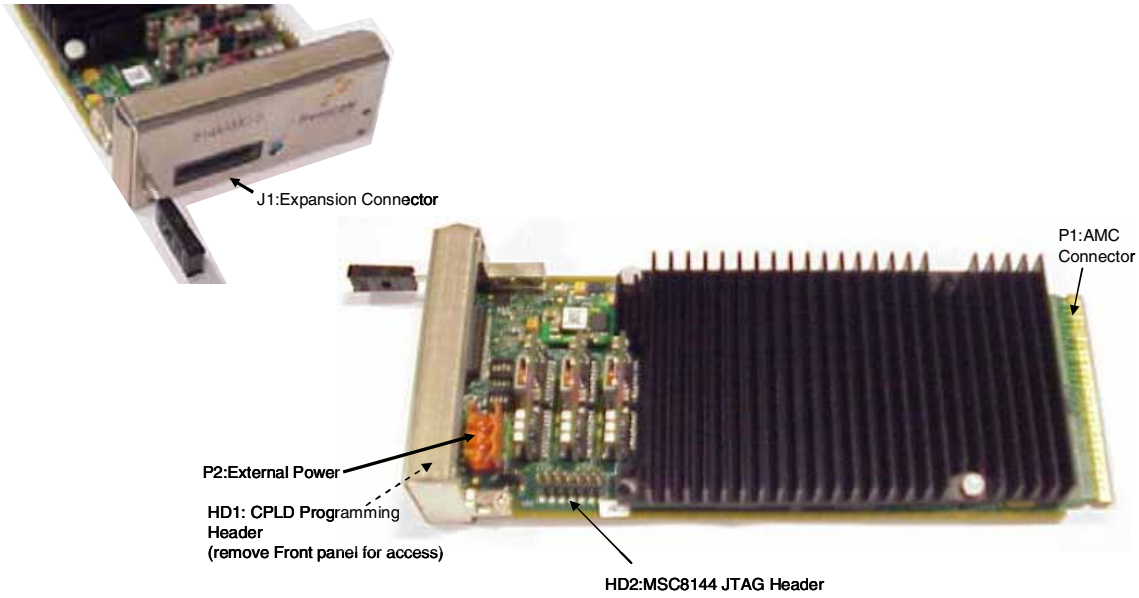


Figure 1-1. MSC8144AMC-S Board External Connections

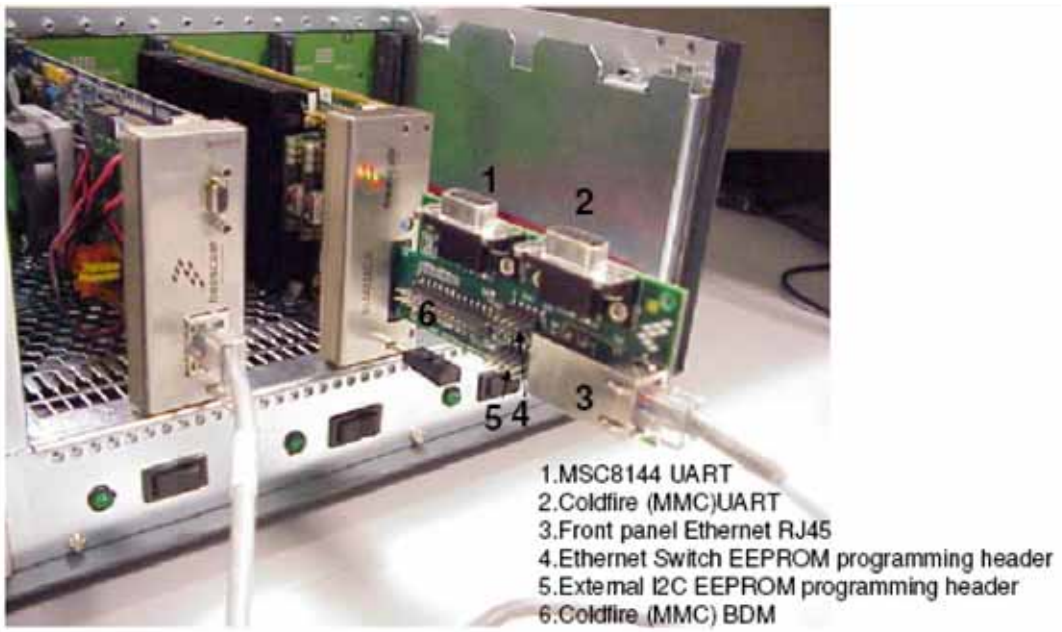


Figure 1-2. MSC8144AMC-S Expansion Card External Connections

1.4 MSC8144AMC-S Block Diagram

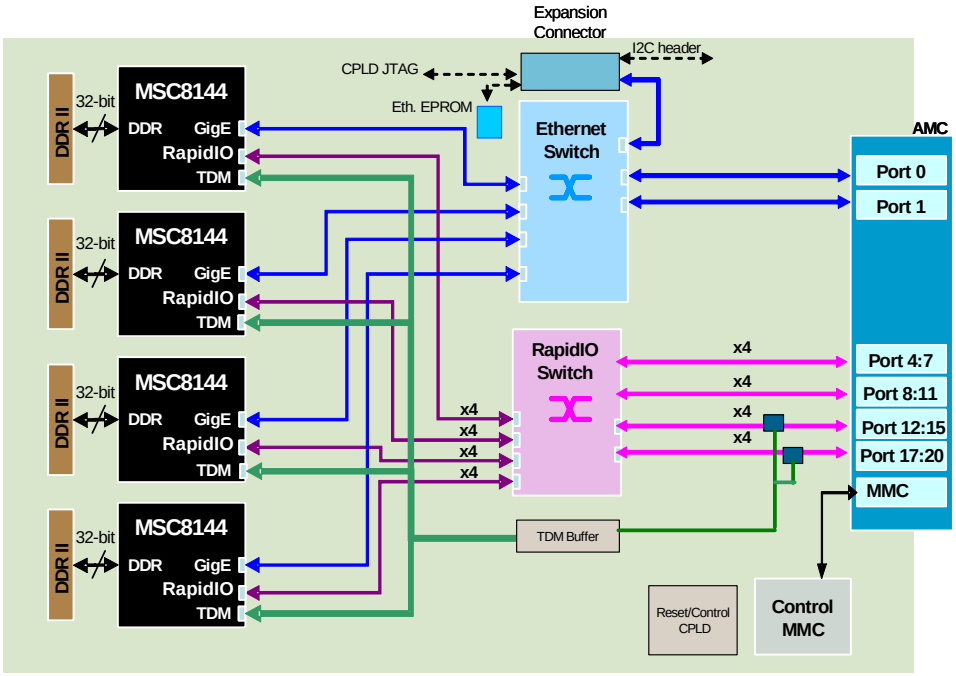


Figure 1-3. MSC8144AMC-S Block Diagram

1.5 Definitions, Acronyms, and Abbreviations

Table 1-1. Definitions, Acronyms, and Abbreviations

Acronym	Definition
AMC	Advanced Mezzanine Card
ATCA	Advanced Telecommunications Computing Platform
BDM	Background Debug Mode
CPLD	Complex Programmable Logic device
DIP	Dual In Line Package
DNP	Do Not Populate
DSP	Digital Signal Processor
EEPROM	Electrically Erasable, Programmable Read Only Module
GETH	Giga-bit Ethernet
HW	Hardware
I^2C(bus)	inter-IC bus
RCW	Reset Configuration Word
UART	Universal Asynchronous Receiver/Transmitter
UEC	UCC Gigabit Ethernet Controller
uTCA	micro Telecommunications Computing Platform

1.6 Related Documentation

This document references the following documents:

- MSC8144AMC-S Getting Started Guide
- MSC8144 Reference Manual
- MSC8144 Data Sheet
- PICMG AMC.0 R2.0 “Advanced Mezzanine Card Base Specification”
- PICMG 2.15 “PCI Telecom Mezzanine/Carrier card Specification”

1.7 Specifications

Table 1-2 specifies the board physical characteristics. Table 1-3 specifies the DSP processing support.

Table 1-2. MSC8144AMC-S Board

Characteristics	Specifications
Power Requirements	No external power supply for AMC modes- powered from ATCA Carrier / uTCA Chassis In standalone mode, the recommended PSU should supply 12 V at 5 A, and 3.3 V at 150 mA
Operating temperature	0° C to 70° C
Storage Temperature	–25° C to 85° C
Relative humidity	5% to 90% (non condensing)
Dimensions	Single width AMC form factor Length = 180.6 mm Width: 73.5 mm Thickness: 1.6 mm

Table 1-3. Processing Support

Subsystem	Component	Specifications
MSC8144 DSPs	Cores per DSP	4 cores each running at 1 GHz
Memory	Internal M2, M3	Total 10.96 Mbytes
	External DDR	256 Mbytes of 32-bit wide DDR2-400
	I^2C EEPROM	64-Kbyte serial EEPROM for Boot Code
Communication Ports	Gigabit Ethernet	RGMII GigE DSP to switch SerDes from switch to backplane/frontplane
	Serial RapidIO Interface	x1/x4 serial RapidIO protocols. Hardware-configurable to 1.25 GHz, 2.5 GHz, and 3.125 GHz data rates
	TDM	Eight TDM ports shared between DSPs and routed to the backplane via optional DNP resistors
	UART	RS-232 transceiver allows data exchange at 115 Kbps

Chapter 2
Hardware Preparation and Installation

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MSC8144AMC-S Processor Board. For details on hardware preparation, see the *MSC8144AMC-S Hardware Getting Started Guide* (MSC8144AMCSHWGSG).

2.1 Unpacking Instructions

NOTE

If the shipping carton is damaged upon receipt, request that the carrier agent to be present during unpacking and inspection of equipment.

CAUTION

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

- Unpack equipment from shipping carton
- Refer to packing list and verify that all items are present
- Save packing material for storing and reshipping of equipment

2.2 Installation Instructions

Perform the following steps in the order listed to install the MSC8144AMC-S Processor Board properly.

1. Verify that jumpers and switches are in their default positions (See Chapter 4, "Controls and Indicators," for a list of default positions).
2. Connect external cables in accordance with your needs (See Section 1.3.2, "External Connections," for more details).
3. Insert the board into the carrier/chassis as per the specific chassis operating instructions.
4. Switch on the power to the chassis.
5. Check for completion of the reset sequence indicated by the LEDs; see Figure 4-1 for locations. A full description of the LEDs is given in Table 4-3.
6. When powered up, verify that the 12 V (LD601) and 3.3 V (LD602) LEDs illuminate and stay lit. This indicates the board power is applied.
7. Check for completion of the reset sequence by verifying the following LEDs:
   a) Verify the DSP PORESET (LD609) and PORESET (LD612) LEDs illuminate and then turn off to indicate that the MSC8144 reset sequence is complete.
   b) The four MSC8144 RGMII Activity LEDs (LD610, LD606, LD607, LD608) illuminate and then turn off.
8. Ethernet port activity LEDs (LD614, LD615) indicate any Ethernet link to the backplane (system-dependent).
9. Pressing the front panel reset button SW1 power-cycles the board and starts the reset sequence.
10. Pressing the reset button SW2 resets the board and starts the reset sequence
11. Operate the CodeWarrior IDE software to verify that the board is installed properly

Chapter 3
Memory Map

Each of the four MSC8144s has an identical memory map as described in Table 3-1.

Table 3-1. MSC8144 Memory Map

Address Range	Memory Type	Device Name	Size
0x40000000–0x4FFFFFFF	External DDR2	2x 16-bit wide MT47H64M16HR	256 Mbytes
0x50000000–0xBFFFFFFF	—	Empty space	1.5 Gbytes
0xC0000000–0xC007FFFF	M2 Shared	Internal	512 Kbytes
0xC0080000–0xC007FFFF	—	Empty space	255.5 Mbytes
0xD0000000–0xD09FFFFF	M3 memory	Internal	10 Mbytes
0xD0A00000–0xDFFFFFFF	—	Empty space	1 Gbyte
0xE0000000–E7FFFFFF	PCI Port	Internal (PCI not used)	128 Mbytes
0xE8000000–0xFEDFFFF	—	Empty space	366 Mbytes
0xFEE00000–0xFEE3FFF	QUICC Engine subsystem	Internal	256 Kbytes
0xFEE40000–0xFEEFFFF	—	Empty Space	768 Kbytes
0xFEF00000–0xFEF17FFF	Boot ROM	Internal	96 Kbytes
0xFEF18000–0xFFFFFFFF	—	Empty Space	928 Kbytes

Chapter 4
Controls and Indicators

This chapter describes the controls and indicators for the MSC8144AMC-S processor board, which includes switches, jumpers, LEDs, and push button switches shown in Figure 4-1.

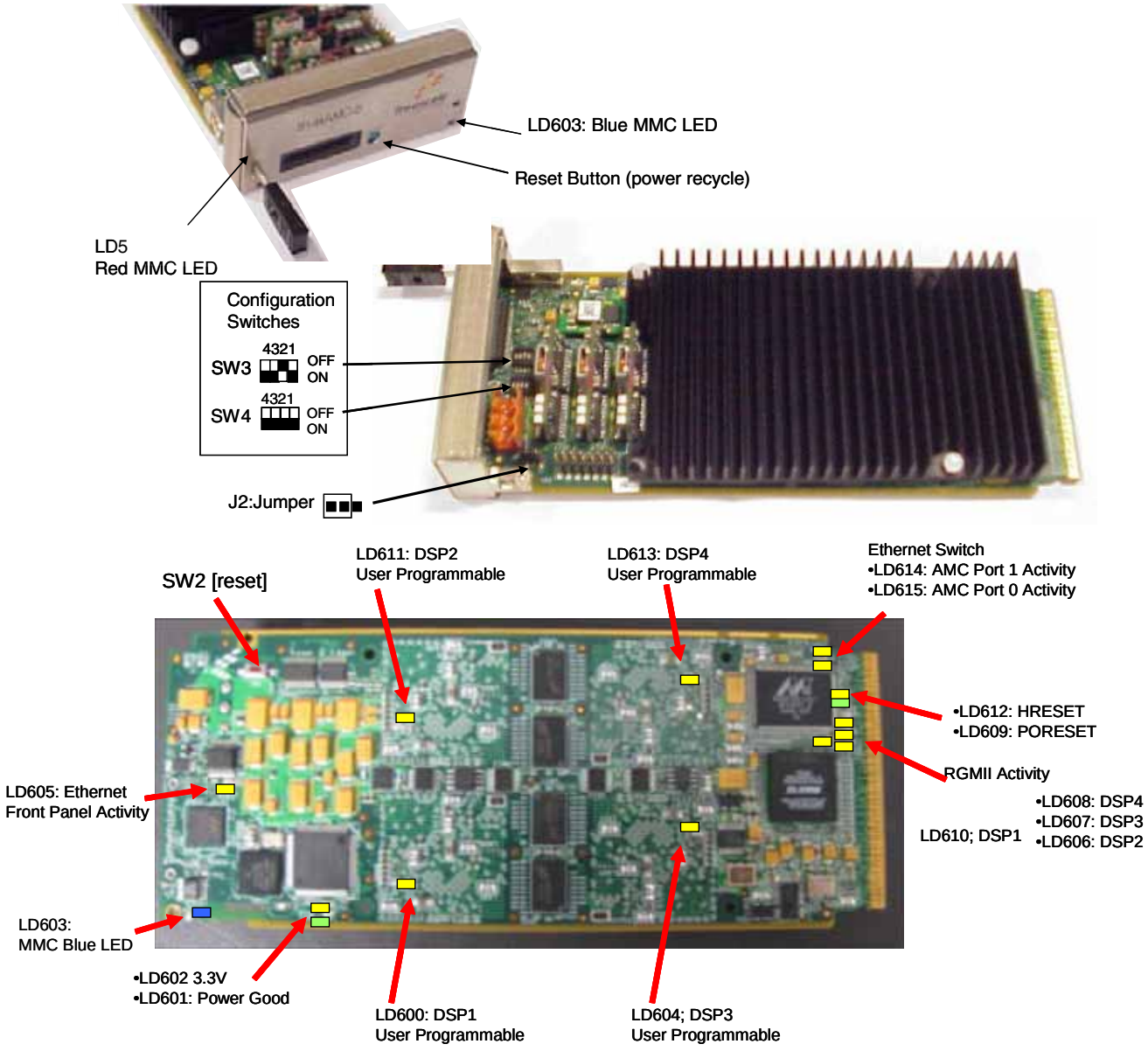


Figure 4-1. MSC8144AMC-S Switches, Jumpers, LEDs, and Push Buttons Locations

4.1 DIP Switches

Figure 4-1 shows the location on the board of the DIP switches in their default position. Figure 4-2 describes the possible settings of the switches. Note that when ON, the value of the switch is zero. For a detailed description of the bits and fields see the *MSC8144 Reference Manual*. Check the default positions and make sure that the board is operational before changing any settings.

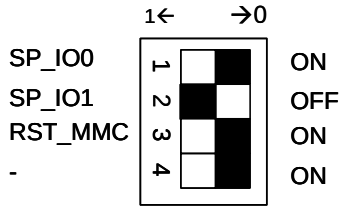
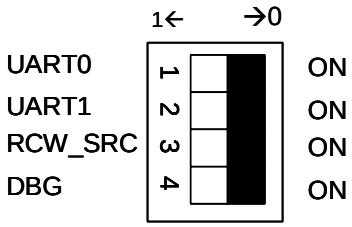
SW3 Configuration  	SW3.1-SW3.2 SP_IO_SPEED[0:1]: Select TSI578 SRIO Speed 00 = 1.25 GHz 01 = 3.125 GHz [Default] 10 = 2.5 GHz 11 = illegal SW3.3 0 = Reset CPLD controlled Power Up [default] 1 = ColdFire device-controlled MMC SW4.4 Future use
SW4 Configuration  	SW4.1-SW4.2 Select MSC8144 UART output 00 = DSP1 [default] 01 = DSP2 10 = DSP3 11 = DSP4 SW4.3 0 = RCW Source from I2C pins/Boot Port = Serial RapidIO interface[default] 1 = RCW Source from External pins /Boot Port = I^2C SW4.4 0 = MSC8144 does not enter Debug Mode but operates normally [default] 1 = MSC8144 enters Debug Mode after reset, see MSC8144 Reference Manual for details.

Figure 4-2. DIP Switch Settings

Table 4-1. MSC8144AMC-S Clock Values

Ref Clock	SW4.3 = ON	SW4.3 = OFF
CLKIN	66 MHz	66 MHz
Cores	1 GHz	800 MHz
System Clock	400 MHz	400 MHz
M3	400 MHz	400 MHz
DDR	400 MHz	400 MHz
QUICC Engine	400 MHz	400 MHz
Serial RapidIO	3.125 GHz	1.25 GHz

4.2 Jumpers

There is one jumper on the board, described in Table 4-2, that is used to configure the CPLD JTAG chain.

Table 4-2. Jumper Position

Jumper	Description
J2	Selects the Reset and System JTAG Chain • When in position 1-2 the Reset CPLD only is in the chain • When in position 2-3 both the Reset and System CPLDs are in the chain **Note:** If the reset CPLD is blank then use position 1-2 to program the Reset CPLD

4.3 LEDs

Table 4-3 describes the LED functions and Figure 4-1 shows the LED location on the MSC8144AMC-S Processor Board.

Table 4-3. LED Descriptions

No.	Description	Color	LED On	LED Off
LD601	Power Good	Green	Power good	Power supply fail(*)
LD602	3.3 V (IPMCV) present	Yellow	IPMCV power on	IPMCV power off
LD609	PORESET	Green	PORESET asserted	PORESET de-asserted
LD612	HRESET	Yellow	HRESET asserted	HRESET de-asserted
LD600	DSP1 User Programmable	Yellow	User programmable	User programmable
LD611	DSP2 User Programmable	Yellow	User programmable	User programmable
LD604	DSP3 User Programmable	Yellow	User programmable	User programmable
LD613	DSP4 User Programmable	Yellow	User programmable	User programmable
LD610	DSP1 RGMII Activity	Yellow	Ethernet activity	No Ethernet activity
LD606	DSP2 RGMII Activity	Yellow	Ethernet activity	No Ethernet activity
LD607	DSP3 RGMII Activity	Yellow	Ethernet activity	No Ethernet activity
LD608	DSP4 RGMII Activity	Yellow	Ethernet activity	No Ethernet activity
LD605	Front Panel Ethernet Activity	Yellow	Ethernet activity	No Ethernet activity
LD615	AMC Port 0 Ethernet Activity	Yellow	Ethernet activity	No Ethernet activity
LD614	AMC Port 1 Ethernet activity	Yellow	Ethernet activity	No Ethernet activity
LD603	MMC Blue LED (Hot swap)	Blue	Hot swap mode	Non-hot-swap mode
LD5	MMC Red LED (Status	Red	Fault condition	Normal operation.

(*) Critical Indicator

4.4 Push Buttons

Figure 4-3 describes the MSC8144AMC-S Processor Board push buttons.

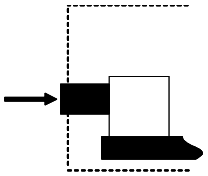
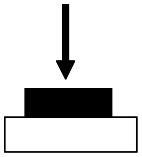
SW1 Power Cycle		Pressing button SW1 on the front panel recycles the board power (Restarts the power sequencing on the board.)
SW2 Hard Reset		Pressing button SW2 on the back of the board causes a Power On Reset to all Components.

Figure 4-3. MSC8144AMC-S Push button Switches

Chapter 5
MSC8144AMC-S Functional Description

This chapter describes the design details of the various MSC8144AMC-S hardware blocks. The hardware description has been partitioned into the following logical sections:

- MSC8144 Digital Signal Processing Block
- MSC8144 to Backplane SRIO Connectivity
- MSC8144 to Backplane Ethernet Connectivity
- Board Control (Power, Reset, Clock, JTAG and others)

The MSC8144AMC-S is designed to comply with the PICMG AMC.0 R2.0 specification with AMC.4 (serial RapidIO interface), fitting into a single-width, full height mezzanine card. The card contains four MSC8144 devices with associated DDR2 memory. Each MSC8144 has gigabit Ethernet connectivity to the AMC backplane via an Ethernet switch. There is serial RapidIO connectivity to the backplane via a serial RapidIO switch. In addition, 32 TDM lines (16 Rx and 16 Tx) are routed to the backplane from each DSP. All eight TDM Modules, with two links per module, are connected together over a common bus, to achieve 32 TDM lines. For bootstrap purposes a common serial I^2C bus is connected between the devices with an I^2C EEPROM hanging of the bus. The programming of the EEPROM is through the master MSC8144 or through an in-circuit programmer attached to a header on the I^2C bus.

5.1 MSC8144 Digital Signal Processing Block

The MSC8144 Digital Signal Processing Block consists of four MSC8144s, DDR2, and associated interfaces. In the design DSP1 is referred to as the master managing the bootstrap of itself and the three slave devices. The three slave devices are all identical.

5.1.1 MSC8144 DDR2 Memory

Each MSC8144 integrates a DDR2 controller and is provided with 32-bit-wide, 256-Mbyte external DDR2 SDRAM. The memory is constructed with two 400 MHz, 8 Mbytes x 16 bits x 8 banks (512-Mbit) DDR2-SDRAM devices (200 MHz external clock). The DDR2-SDRAM is configured with 13 row address lines, 10 column address lines, and 8 banks. Control of each memory is via the CS0 signal. Individual differential clocks and their associated enable signal are routed to each memory. EEC is not supported in this configuration and the unused signals are pulled high/low. The physical mapping of the signals is shown in Figure 5-1.

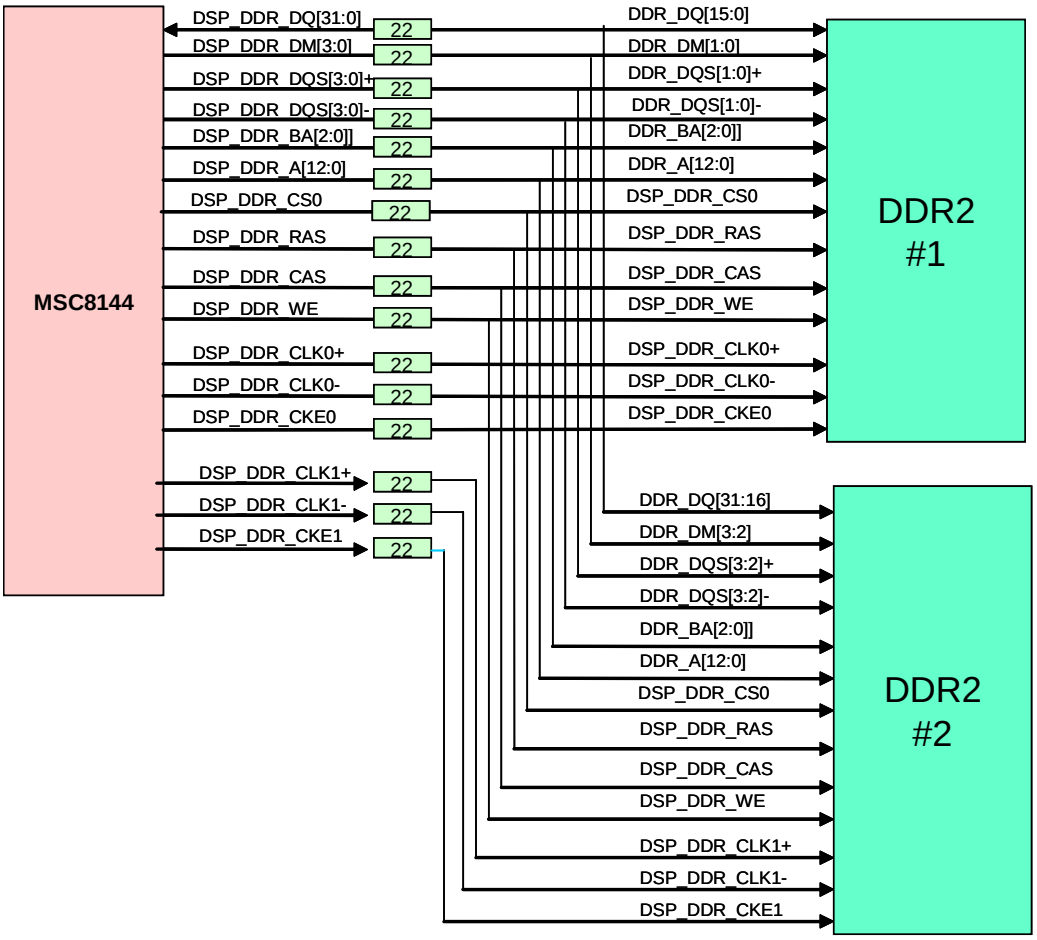


Figure 5-1. DDR2 Connectivity

5.1.1.1 DDR Groups

Every DDRII signal can be considered to be a member of one of four separate groups. Each group has unique rules in terms of signal connection and signal routing. The four groups are shown in Table 5-1.

Table 5-1. DDR2 Interface Signals

Signal Group	Signal	Description
Address and Command	MA[12:0]	Address bus
	MBA[3:0]	Bank Address Bus
	MWE	Write Enable
	MCAS	Column Address Strobe
	MRAS	Row Address Strobe
Control	MCKE[1:0]	Clock Enable
	MCS0	Chip Select
	MODT[1:0]	On-Die Termination
Data	MDQS[3:0]+	Data Strobes
	MDQS[3:0]-	Data Strobes Complement
	MDM[3:0]	Data Mask
	MDQ[31:0]	Data Bus
	MECC[3:0]	Error Correction bits
Clocks	MCK[1:0]+	Clock
	MCK[1:0]-	Clocks Complement

Complex DDR2 timing adaptation is available via the DDR clocking subsystem of the MSC8144. It supports the following:

- Positioning of the DQS output during writes to DDR memory
- Sampling of input data from DDR memory
- Synchronize the incoming DDR data to the Internal Clock
- Control the relationship between output data and CLK_OUT

5.1.1.2 Terminations and I/O Voltage

The DDR2 interface operates with 1.8 V I/O voltages. Reference voltages of 0.9 V are synthesized from the 1.8 V via filtered 2:1 voltage dividers (2x1-Kbyte resistors) with low impedance to the 1.8 V supply. The references are applied to each DDR2 device (at VREF pin) and the MSC8144 (at pin MVREF).

Because the device fan out is low (FO = 2 Data, 2 Address, 2 Control) and the clock frequency is relatively low for DDR2 (200 MHz), the MSC8144 and DDR2 devices can be programmed for reduced power using a series termination scheme. In addition to the benefits of the power/heat, series termination allows the removal of a 0.9 V regulator from the design.

5.1.2 MSC8144 Serial RapidIO Interface

The RapidIO® controller supports a high-performance, point-to-point, low pin count packet, switched-level interconnect that can be used in a variety of applications as an open standard. The MSC8144 serial RapidIO subsystem complies with the RapidIO Interconnect Specification Revision 1.2, which connects directly to a serial RapidIO switch. Each port in the switch is point-to-point connected to the MSC8144 device through a serial RapidIO link. The MSC8144 routes the serial RapidIO interface to the backplane via the Tundra TSI578 serial RapidIO switch, as shown in Figure 5-2. The interface can work in x1 or x4 mode and is selectable. The signals are detailed in Table 5-2.

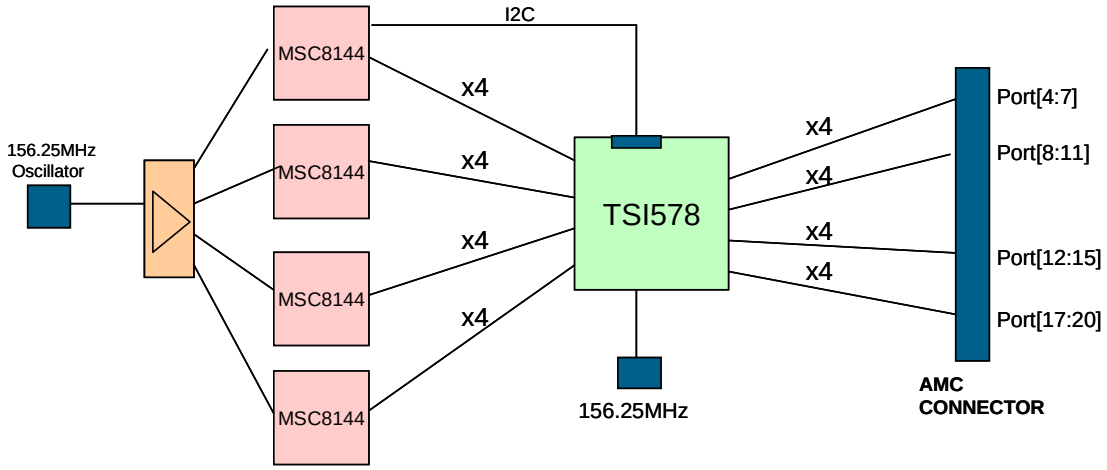


Figure 5-2. Serial RapidIO Connectivity

Table 5-2. MSC8144 Serial RapidIO x4 Signals

Signal	Description
SRIO_TXD_P[0:3]	Transmit +ve differential signal
SRIO_TXD_N[0:3]	Transmit -ve differential signal
SRIO_RXD_P[0:3]	Receive +ve differential signal
SRIO_RXD_N[0:3]	Receive -ve differential signal
DSP_SD_REFCLK_P	156.25MHz differential +ve Clock
DSP_SD_REFCLK_N	156.25MHz differential -ve Clock

Both the MSC8144 and TSI578 run with a fixed clock frequency of 156.25 MHz. The transmission frequency of the MSC8144 serial RapidIO interface is dependent on the Reset Configuration Word SCLK bits. The various options are described below in Table 5-3. The default setting is to run at 3.125 GHz using the 156.25 MHz clock. One restriction when booting from external pins is that the clock must be 100 MHz for 1.25 GHz.

Table 5-3. MSC8144 RapidIO Settings

RapidIO	Ref. Clock	RCWLR[SCLK]	Boot Mode
1.25 GHz	100 MHz	001	RCW from external Signals (RCW_SRC=011)
2.5 GHz	156.25 MHz	101	RCW from I^2C (RCW_SRC=001)
1.25 GHz	156.25 MHz	110	RCW from I^2C (RCW_SRC=001)
3.125 GHz	156.25 MHz	111 [Default]	RCW from I^2C (RCW_SRC=001)

5.1.3 MSC8144 Ethernet Interface

The MSC8144 supports two UCC Gigabit Ethernet Controllers (UECs) coordinated through the QUICC Engine Controller. On the MSC8144AMC-S, the MSC8144s are configured to use the RGMII interface. This UEC interface selection is restricted to RGMII because of the requirements for x4 serial RapidIO signals which use the SGMII pins.

5.1.3.1 Ethernet Connections

Each MSC8144 connects its RGMII Ethernet port to the Marvell 88E1145 Ethernet transceiver, which performs RGMII to SGMII conversion. A 10-port Marvell 88E6185 SGMII Ethernet switch then switches between the MSC8144s and the 1000Base-X “Common Option Ports 0 and 1” at the AMC connector. Additionally, one port of the Ethernet switch is connected to a front plane Ethernet port through a Marvell 88E1111. Due to PCB space restrictions, the RJ45 connector is located on the expansion connector.

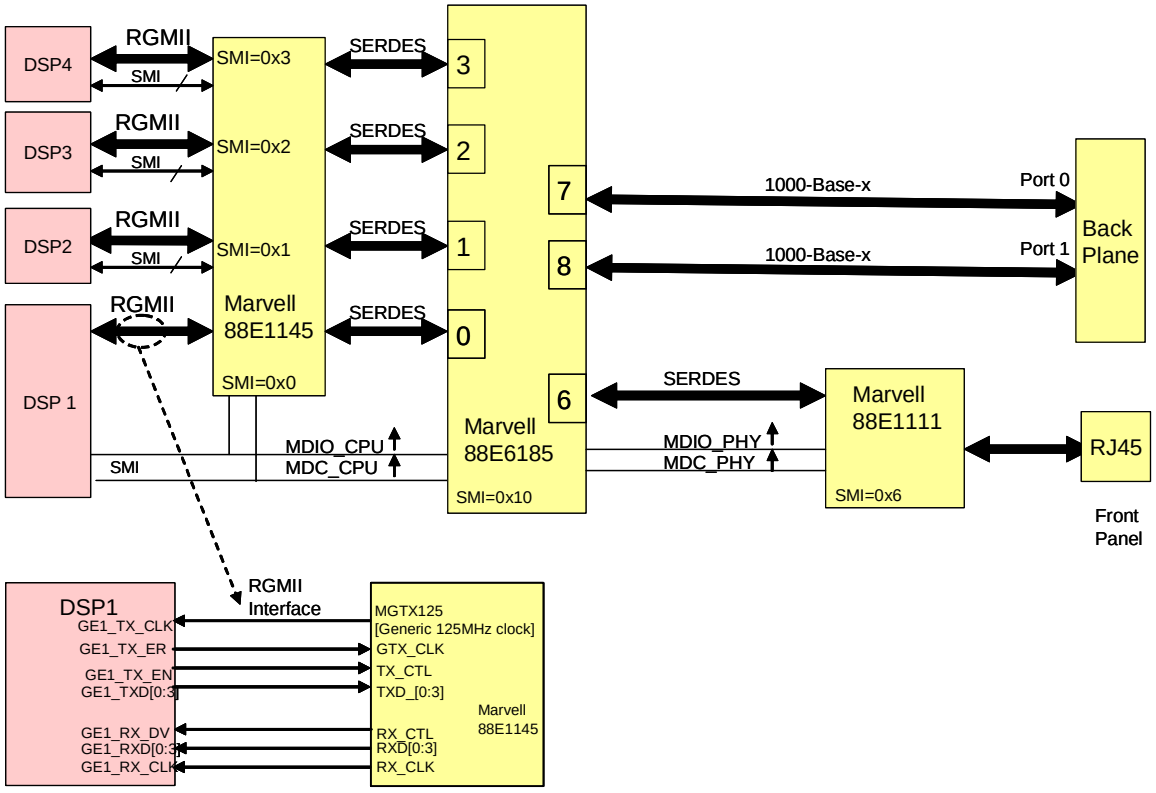


Figure 5-3. Ethernet Hardware Block

The MSC8144 UEC1 interfaces to a Marvell 88E1145 Quad PHY device connecting to each of the four ports. Table 5-4 describes the signals.

Table 5-4. MSC8144 RGMII Signals

Signal	Description
GE1_TX_CLK	125 MHz clock source
GE1_TX_ER	Transmit clock
GE1_TX_EN	Transmit Control
GE1_TXD[0:3]	Transmit data
GE1_RX_CLK	Receive clock
GE1_RX_DV	Receive Control
GE1_RXD[0:3]	Receive data
MDC	Management data clock
MDIO	Management data

5.1.3.2 Ethernet Initialization

Each DSP has a MDIO connection to the 88E1145 QPHY, enabling each DSP to independently configure its own 88E1145 port. DSPs 1, 2, 3, and 4 have been given the SMI address 0, 1, 2, and 3, respectively. DSP1 configures the Ethernet switch, which resides at address 0x10. The switch contains a PHY Polling Unit (PPU), which transfers link, speed, duplex, and pause information from the 88E1111 to the switch. For this feature to function, the 88E1111 SMI address (0x6) matches the switch port that it is connected to (Port 6).

5.1.4 MSC8144 TDM Interface

Each MSC8144 TDM interface is routed to the AMC edge connector via a common open drain bus through a CPLD, as shown in Figure 5-4. The TDM modules on the MSC8144s are configured in Common Frame and Sync mode.

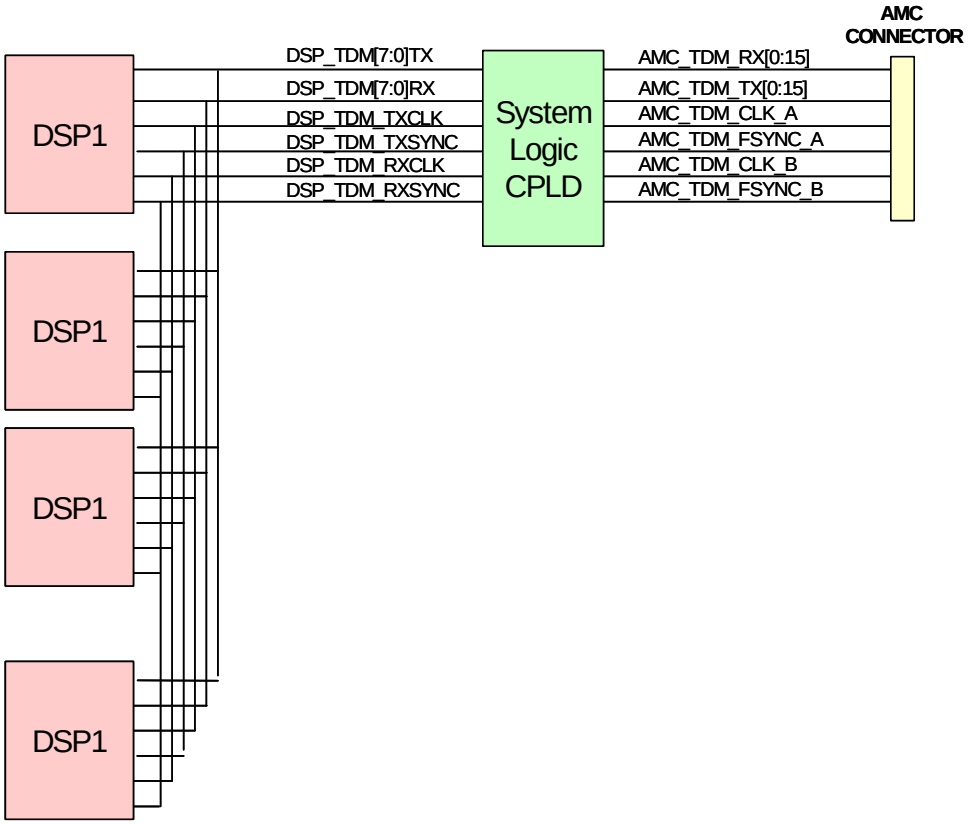


Figure 5-4. TDM Routing

The TDM routing to the AMC connector is configured as 32 TDM lines (16 Tx and 16 Rx) with frame sync and clock. This is a proprietary connection to the extended options section of the AMC connector. It is designed to match the interface on the Freescale Torridon2 ATCA carrier. The TDM signals themselves are multiplexed with two x4 serial RapidIO streams at the backplane connector. The selection between the serial RapidIO interface and TDM interface on this proprietary interface is made via “Do Not Populate” zero Ω resistors. Typically this populate/no-populate option is carried out during assembly. The default is for the TDM option not to be populated; see Figure 5-5.

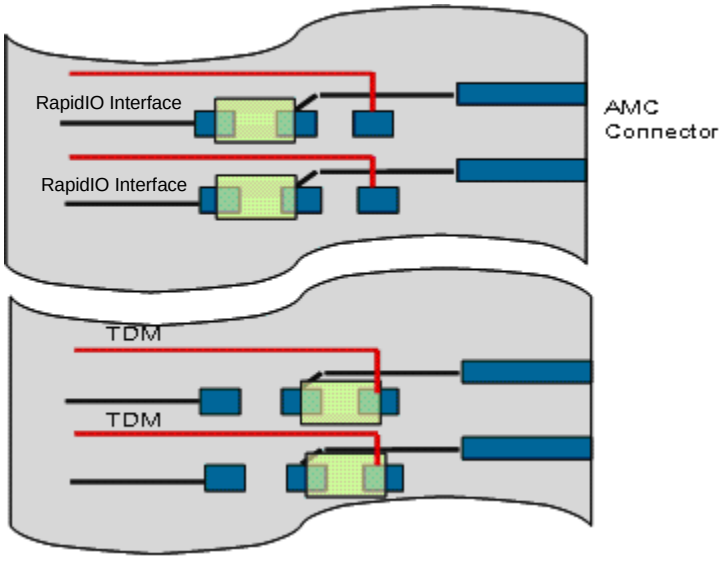


Figure 5-5. Zero Ohm Resistor Selection for TDM or Serial RapidIO Interfaces

Table 5-5 details the end-to-end TDM connectivity on the AMC Card.

Table 5-5. TDM Connectivity on AMC Card and CPLD Mapping

AMC Connector Pin Name	AMC Connector Pin Number	AMC Side		DSP Side		DSP Pin	DSP Pin Name
		CPLD Pin Number	CPLD Net Name	CPLD Pin Number	CPLD Net Name		
TX20+	163	J5	AMC_TDM_CLK_A	F4	DSP_TDM_TXCLK	AG3	TDM0TCLK
TX20-	162	J12	AMC_TDM_FSYNC_A	E5	DSP_TDM_TXSYNC	AF5	TDM0TSYN
RX20+	160	K5	AMC_TDM_CLK_B	F6	DSP_TDM_RXCLK	AD6	TDM1TCLK
RX20-	159	K6	AMC_TDM_FSYNC_B	F5	DSP_TDM_RXSYNC	AE5	TDM1TSYN
TX19+	157	H2	AMC_TDM_RX15	K16	DSP_TDM_RXD15	C4	TDM7RDT
TX19-	156	M1	AMC_TDM_TX15	F15	DSP _TDM_TXD15	C5	TDM7RCK
RX19+	154	G3	AMC_TDM_RX14	L14	DSP _TDM_RXD14	D5	TDM7RSYN
RX19-	153	M4	AMC_TDM_TX14	E13	DSP _TDM_TXD14	D4	TDM7TDT
TX18+	151	G1	AMC_TDM_RX13	K15	DSP _TDM_RXD13	AB4	TDM6RDT
TX18-	150	L2	AMC_TDM_TX13	F16	DSP _TDM_TXD13	AB7	TDM6RCK
RX18+	148	F3	AMC_TDM_RX12	L13	DSP _TDM_RXD12	AC5	TDM6RSYN
RX18-	147	M3	AMC_TDM_TX12	E14	DSP _TDM_TXD12	AC8	TDM6TDT
TX17+	145	G2	AMC_TDM_RX11	L16	DSP _TDM_RXD11	AB5	TDM5RDT
TX17-	144	L1	AMC_TDM_TX11	G15	DSP _TDM_TXD11	AA5	TDM5RCK
RX17+	142	E2	AMC_TDM_RX10	M14	DSP _TDM_RXD10	AA3	TDM5RSYN
RX17-	141	M2	AMC_TDM_TX10	F13	DSP _TDM_TXD10	AA4	TDM5TDT
TX16+	139	F1	AMC_TDM_RX9	L15	DSP _TDM_RXD9	AB9	TDM4RDT
TX16-	138	K2	AMC_TDM_TX9	G16	DSP _TDM_TXD9	Y5	TDM4RCK
RX16+	136	E3	AMC_TDM_RX8	M13	DSP _TDM_RXD8	AB8	TDM4RSYN
RX16-	135	L4	AMC_TDM_TX8	F14	DSP _TDM_TXD8	AA8	TDM4TDT
TX15+	133	F2	AMC_TDM_RX7	M16	DSP _TDM_RXD7	AD9	TDM3RDT

Table 5-5. TDM Connectivity on AMC Card and CPLD Mapping (continued)

AMC Connector Pin Name	AMC Connector Pin Number	AMC Side		DSP Side		DSP Pin	DSP Pin Name
		CPLD Pin Number	CPLD Net Name	CPLD Pin Number	CPLD Net Name		
TX15-	132	K1	AMC_TDM_TX7	H15	DSP _TDM_TXD7	AE8	TDM3RCK
RX15+	130	F4	AMC_TDM_RX6	N14	DSP _TDM_RXD6	AD8	TDM3RSYN
RX15-	129	L3	AMC_TDM_TX6	G14	DSP _TDM_TXD6	AD7	TDM3TDT
TX14+	127	E1	AMC_TDM_RX5	M15	DSP _TDM_RXD5	AF9	TDM2RDT
TX14-	126	J2	AMC_TDM_TX5	H16	DSP _TDM_TXD5	AG8	TDM2RCK
RX14+	124	D2	AMC_TDM_RX4	N13	DSP _TDM_RXD4	AG9	TDM2RSYN
RX14-	123	K3	AMC_TDM_TX4	H14	DSP _TDM_TXD4	AE10	TDM2TDT
TX13+	121	D1	AMC_TDM_RX3	N16	DSP _TDM_RXD3	AF6	TDM1RDT
TX13-	120	J1	AMC_TDM_TX3	J16	DSP _TDM_TXD3	AE4	TDM1RCK
RX13+	118	D3	AMC_TDM_RX2	P15	DSP _TDM_RXD2	AF7	TDM1RSYN
RX13-	117	J3	AMC_TDM_TX2	J14	DSP _TDM_TXD2	AE6	TDM1TDT
TX12+	115	C2	AMC_TDM_RX1	N15	DSP _TDM_RXD1	AF4	TDM0RDT
TX12-	114	H1	AMC_TDM_TX1	J15	DSP _TDM_TXD1	AG5	TDM0RCK
RX12+	112	C3	AMC_TDM_RX0	P14	DSP _TDM_RXD0	AG4	TDM0RSYN
RX12-	111	H3	AMC_TDM_TX0	K14	DSP _TDM_TXD0	AG6	TDM0TDT

5.1.5 MSC8144 UART Interface

The individual DSP UARTs are multiplexed in the system CPLD with a single UART routed to the expansion connector as shown in Figure 5-6. Switch 4 is used to select which UART is routed through the CPLD. The ICL3225 is configured to power down when there is no active signal by connecting the INVALID signal to the FORCE_ON signal. The INVALID signal goes low when no RS232 levels are detected on any transceiver input.

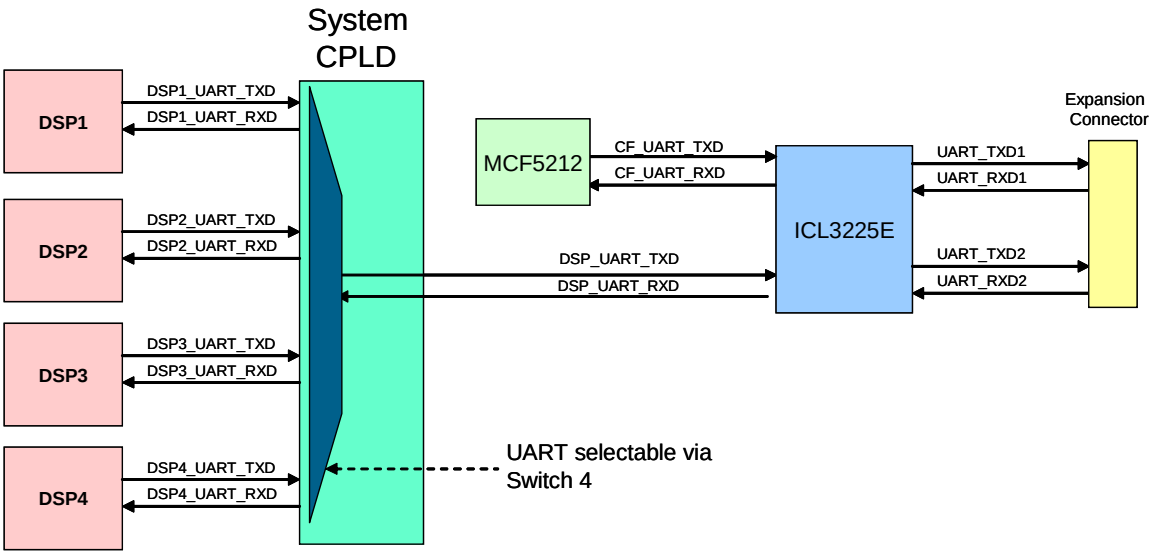


Figure 5-6. UART Connectivity

5.1.6 MSC8144 JTAG Interface

The MSC8144 OCE module allows non-intrusive interaction with the SC3400 core, enabling examination/analysis of registers, memory, and on-chip peripherals. The OCE module connects with the debugging system through on-chip JTAG TAP controller pins as shown in Figure 5-7.

The MSC8144 OCE JTAG debug ports are connected in a chain configuration to allow simultaneous debug of the complete DSP Array. The signals available on the JTAG connector are as follows:

- TMS—This signal is pulled up so that after reset 5 TCK clocks put the TAP into the Test Logic Reset State.
- $\overline{\text{TSRT}}$—The Reset signal is pulled low to force the JTAG into reset by default.
- TCK—The clock signal is pulled low to save power in low power stop mode.
- TDI—The input signal is pulled high to save power in low power stop mode. All JTAG ports have a weak internal TDI pull up.
- TDO—The output signal is pulled high.
- $\overline{\text{HRESET}}$—This signal is pulled high and also connects to the Reset CPLD.

The JTAG control signals are buffered into two sets of signals each supplying two MSC8144s. This reduces device and cable loading of the signals. The JTAG $\overline{\text{TRST}}$ signal is buffered via an open drain buffer with individual signals being fed to the DSPs.

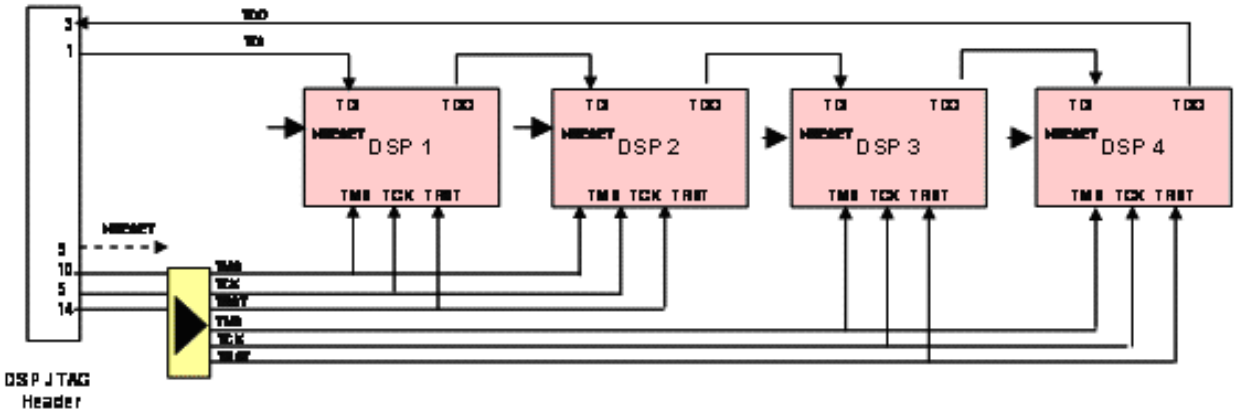


Figure 5-7. MSC8144 JTAG Connections

For debugging, there are a number of zero resistors in the JTAG chain to allow isolation of either of the MSC8144s (not shown in Figure 5-7).

5.1.7 Reset Configuration

The MSC8144 has three external reset sources: Power on Reset ($\overline{\text{PORESET}}$), Hard Reset ($\overline{\text{HRESET}}$), and Soft Reset ($\overline{\text{SRESET}}$). The soft reset is not used in the system and is pulled high. The reset control for all devices is described in Section 5.5.1, "Reset Operation and Connectivity ."

$\overline{\text{PORESET}}$ is the high-level reset of the MSC8144, and when asserted, drives all other resets within the DSP. The rising edge of $\overline{\text{PORESET}}$ is used by the MSC8144 to latch external Reset Configuration Word (RCW) signals.

The Reset Configuration Words Source (RCW_SRC[0:2]) options enable the MSC8144 to load the 32-bit Reset Configuration Word from a variety of sources. Table 5-6 lists the RCW sources on the MSC8144AMC-S card. Note that this is a subset of available device resources. The two options below are selectable via switch 4.

Table 5-6. RCW Sources

RCW_SRC_0:2]	Description
001	Load RCW from I^2C using a frequency specified by RCFG_CLKIN_RNG
011	RC[0:16] loaded from external pins, RC[17:31] are default

Loading the RCW from I^2C allows a different value for each MSC8144 while loading from external pins, as shown in Figure 5-8, means each has the same RCW.

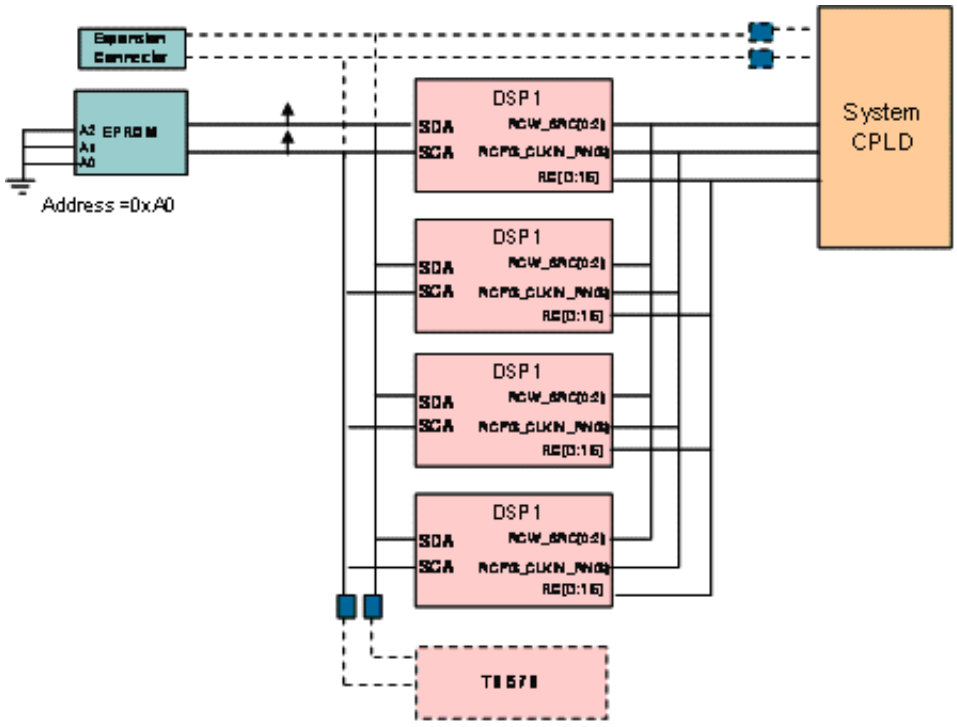


Figure 5-8. Reset Configuration from I^2C

5.1.7.1 Loading Reset Configuration Word from External I²C

When the RCW from I²C is selected, the board powers up and samples the RCW_SOURCE pins and reads 001 for I²C boot, as shown in Table 5-7. The MSC8144 then accesses the I²C bus at address B[7:0]= b1010000, which represents the EPROM. Bits B[7:4] = b1010 are hard coded into the EPROM device, while the bits B[3:1] are defined by the A[2:0] pins, which are tied low. The final bit B0 is set by the read/write signal.

Table 5-7. EEPROM Address

Signal				A[2:0] pins			R/Wn
B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

After the master MSC8144 (DSP1) has read its RCW, it configures itself as a slave EEPROM using the address b1010111. The slaves DSPs (DSP2, 3, 4) then access DSP1 to read their RCW. The EPROM is clocked at 66 MHz so the CNG_CLKIN_RNG is set to 0 via the System Logic CPLD for a CLKIN range of 0–66 MHz. The I²C EPROM can be programmed via DSP1, the expansion header, or the system CPLD. Table 5-8 and Table 5-9 list the I²C layout as programmed in the EPROM.

NOTE

The RCW can be changed depending on the user requirements. The values below represent the default values programmed in the I²C.

Table 5-8. RCWLR (Load from I²C)

RCWLR bit	Name	Value	Description
[31:30]	CLKO	00	Source is CLK2
[29:26]	RES	0000	Reserved
25	SF	0	200 ppm SerDes filter
24	RES	0	Reserved
23	RV	0	Rapid IO V_{DD} Select=1.0V
[22:20]	SCLK	111	RapidIO/SGMII reference clock is 156.25 MHz, serial RapidIO clock is 3.125 GHz
19	RIOE	1	Power is enabled on RapidIO
18	1x/4x	0	Select 4x RapidIO configuration
17	SGMII1	0	Disable SGMII
16	SGMII2	0	Disable SGMII
[15:13]	RES	000	Reserved
12	SPCI	1	Select System PLL
11	SDDR	1	Select System PLL
10	SM3	0	Select System M3
9	RES	0	Reserved
8	GPD	0	Enable Global PLL
7	CPD	0	Enable Core PLL
6	SPD	0	Enable System PLL
[5:0]	MODCK	01010	Mode 10 [1 GHz MSC8144]
DSP1: RCWLR=0x0078180A DSP2: RCWLR=0x0078180A DSP3: RCWLR=0x0078180A DSP4: RCWLR=0x0078180A			

Table 5-9. RCWHR (Load from I²C)

RCW bit High	Name	Value	Description
31	RES	0	Reserved
30	RM	DSP1=1 DSP2=0 DSP3=0 DSP4=0	1: Reset Initiator 0: Reset Target
29	EWDT	0	Disable watch Dog Timer
[28:23]	BPRT	001001	Boot Port = serial RapidIO interface no I²C
22	RES	1	reserved
21	RIO	1	RIO access to internal memory enabled
[20:15]	PTE	011000	Serial RapidIO prescale value = (200 MHz/8) –1
14	RES	0	reserved
[13:10]	PIN_MUX	0001	Pin Mux option 1
[9:4]	DEVID	DSP1=b000000 DSP2=b000001 DSP3=b000010 DSP4=b000011	DSP Device ID
3	Extended Reset	1	Extended reset duration
[2:1]	SLP	00	Normal SerDes operation
0	CTLS	1	Common Transport is large (16-bit) system
DSP1: RCWHR=0x44EC0409 DSP2: RCWHR=0x04EC0419 DSP3: RCWHR=0x04EC0429 DSP4: RCWHR=0x04EC0439			

DSP1, which is designated as the I²C master, controls the STOP_BS pins of the three slave DSPs using GPIO1, 2, 3 as shown in Figure 5-9. DSP1 drives these signals during the I²C boot process, after the DSP exits the reset sequence the signals revert back to standard GPIO.

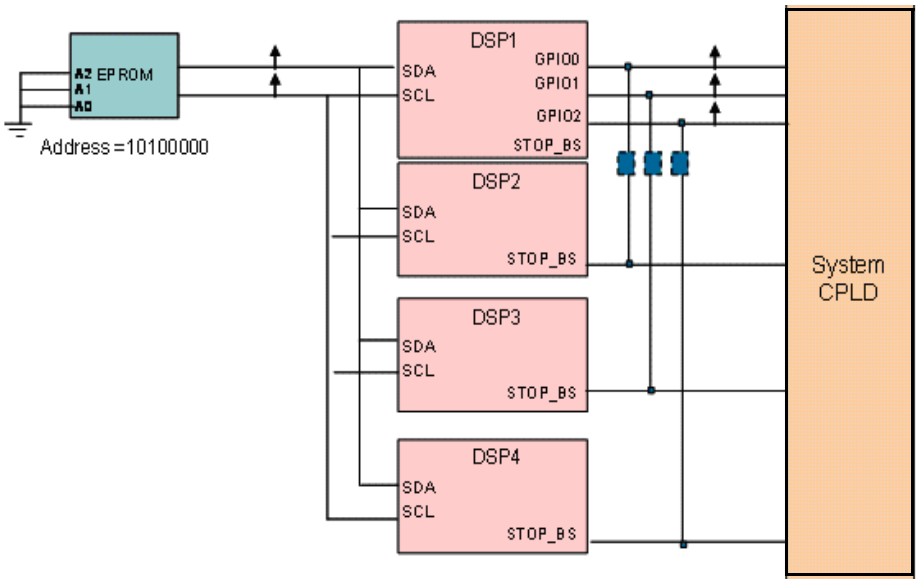


Figure 5-9. I²C Multi-Boot Control

5.1.7.2 Loading Reset Configuration Word from External Signals

This boot option when RCW_SRC[0:2] is read as b011 uses a combination of pins and default values to set the RCW. These values are described in Table 5-10. The RC[0:16] pins are tied together and driven from the System CPLD during Power up. The RCWH and RCWL settings are described in Table 5-10 and Table 5-11. Some values can be changed via the system CPLD, if required.

NOTE

The following restrictions apply when the RCW is loaded from external pins:

The MSC8144 core frequency is 800 MHz. The serial RapidIO interface is restricted to 1.25 GHz data rate with a 100 MHz input frequency. To use this data rate, the user must change the clock (Y602) to 100 MHz.

Table 5-10. RCWLR (Load from External Pins)

RCWLR	Name	Value	Description
[31:30]	CLKO	00	00 = CLK2
[29:26]	RES	0000	Reserved
25	SF	0	SerDes digital filter BW is 200 ppm
24	VCOI	0	SerDes VCO Current reference
23	RV	0	RIO VDD is 1 V
[22:20]	SCLK	001	RIO/SGMII reference clock is 100 MHz, SerDes is 1.25 GBaud
19	RIOE	RC[16] || RC[3] = 1	Serial RapidIO signals enabled on SerDes
18	x4	RC[16] = 0	Serial RapidIO x4 Protocol
17	SGMII1	RC[16] = 0	Disable SGMII 1 on SerDes
16	SGMII2	RC[16] and RC[3] = 0	Disable SGMII 2 on SerDes
[15:13]	RES	000	Reserved
12	SPCI	1	Select System PLL for PCI
11	SDDR	1	Select System PLL for DDR
10	SM3	0	Select Global PLL for M3
9	RES	0	Reserved
8	GPD	0	Enable Global PLLM3
7	CPD	0	Enable Core PLL
6	SPD	0	Enable System PLL
[5:0]	MODCK	000,RC[2:0]= 000	Mode 0 [800 MHz MSC8144]
RCWLR = 0x00181800			

Table 5-11. RCWHR (Load from External Pins)

RCWHR	Name	Value	Description
31	RES	0	Reserved
30	RM	0	No reset Slaves to be configured

Table 5-11. RCWHR (Load from External Pins)

RCWHR	Name	Value	Description
29	EWDT	0	Watchdog Timer disable
28	BPRT[5]	0	Boot Port =001000 I^2C
[27:26]	BPRT[4:3]	RC[15:14]=01	
25	BPRT[2]	0	
[24-23]	BPRT[1:0]	RC[13:12]=00	
22	RES	1	Reserved
21	RIO	1	Serial RapidIO Host Access is enabled
[20:15]	PTE	011000	IO prescale timer enable – OCEAN clock is 200 MHz
14	RES	0	Reserved
[13:10]	PIN_MUX	00, RC[11-10] = 0001	01 – Mode 1 gives TDM[0:7], RGMII
[9:4]	DEVID	RC[9:4]=0000	DSP Device ID
3	RES	0	Reserved
[2:1]	SLP	00	No loopback mode on SERDES
0	CTLS	1	Common Transport type is a Large System
RCWHR=0x046C0401			

5.1.7.3 MSC8144 Clocking

The MSC8144AMC-S implements a point-to-point clocking scheme for the MSC8144s. The CLKIN is a 66-MHz clock distributed through a Zero Delay Buffer. The MSC8144 runs at frequencies of 1 GHz or 800 MHz depending on the RCW source. The default setting is to run the core at 1 GHz using clock mode 10. Figure 5-10 described the internal clocking in the MSC8144.

NOTE

PCI_CLKIN is not used, so all internal frequencies are derived from CLKIN.

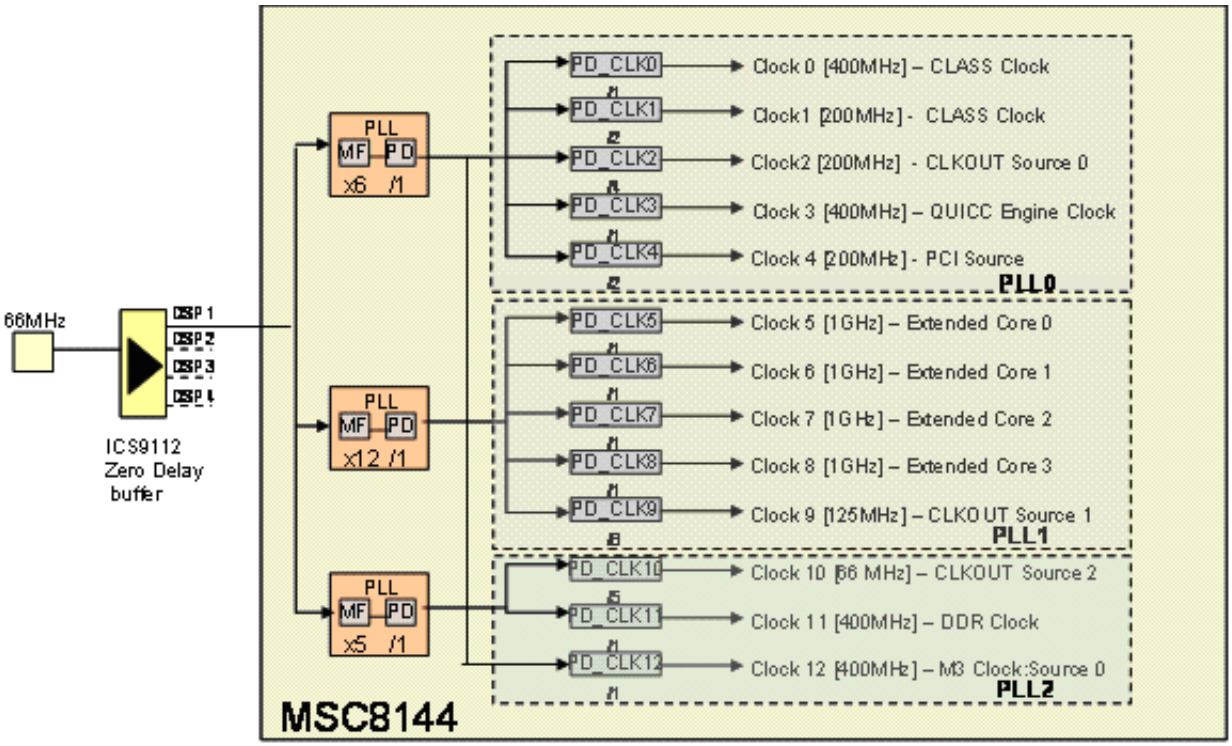


Figure 5-10. MSC8144 Clocking

5.1.8 GPIO/$\overline{\text{IRQ}}$ Distribution

Each DSP on the MSC8144AMC-S connects several multiplexed pins to the system logic CPLD. The pins chosen can be configured as Timers, Interrupts, or GPIO. This enables the MSC8144s to generate interrupts (to each other) and receive a timer input from the system logic. In addition, each DSP routes its dedicated $\overline{\text{INT\_OUT}}$ pin to the system logic CPLD providing lower overhead interrupt generation. Table 5-12 and Figure 5-11 illustrate the implementation. The configuration can be changed by the user through System CPLD logic.

Table 5-12. GPIO/$\overline{\text{IRQ}}$ Options

MSC8144 Pin	Mux Options	Default Configuration	Description
AD3	GPIO13/Timer0	Timer0	Can be connected to AMC clocks via CPLD
AG2	GPIO16/$\overline{\text{IRQ0}}$	$\overline{\text{IRQ0}}$	Interrupt input to the DSP
L3	GPIO17/Timer1	GPIO17	Timer Input
L6	GPIO18/Timer2	GPIO18	Can be used to assert an interrupt to other DSPs via the CPLD.
J6	$\overline{\text{INT\_OUT}}$	$\overline{\text{INT\_OUT}}$	Low overhead Interrupt output

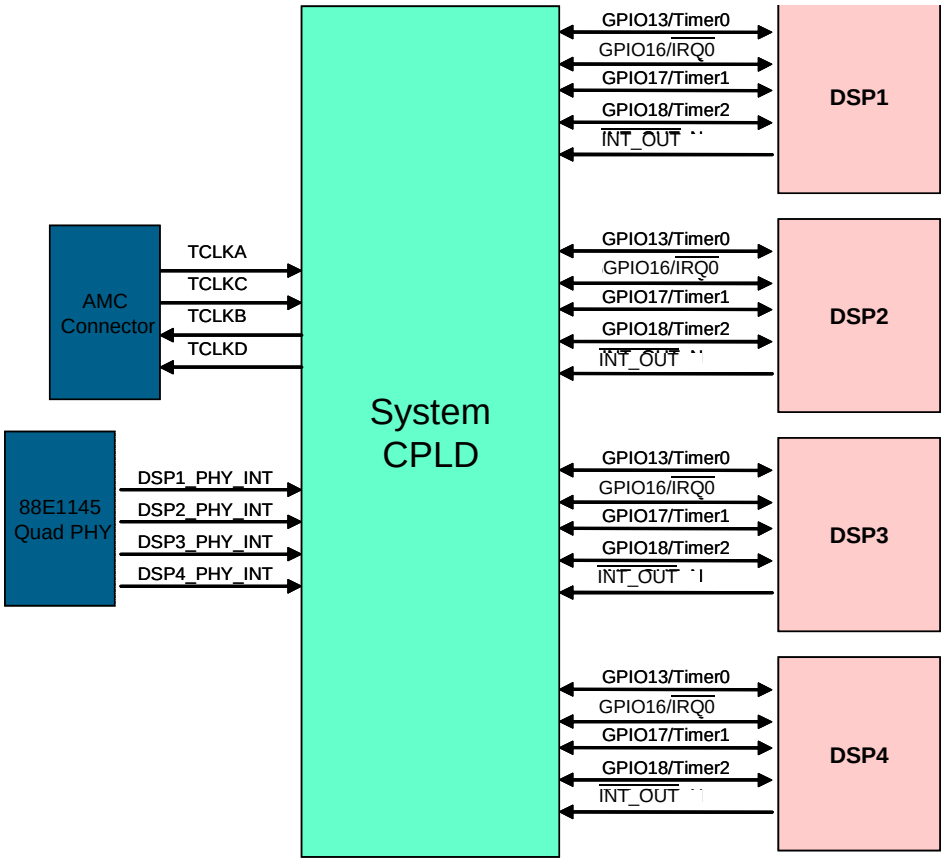


Figure 5-11. MSC8144 $\overline{\text{IRQ}}$/Timer Resources

5.1.9 SPI Interface

The SPI bus connects between the Ethernet Switch, configuration EEPROM, DSP 1, and expansion connector, and is used to program the Ethernet Switch during the reset phase. This gives the user various EEPROM programming options. The default programming interface is to program the EEPROM via a header on the expansion card. This header is pinned out to allow connection to an in-circuit programmer (ICP) driven from a PC (for example, Kanda Serial EEPROM Programmer). Note that the header provides a reset signal that is used to hold the DSPs in Reset whilst programming from the ICP.

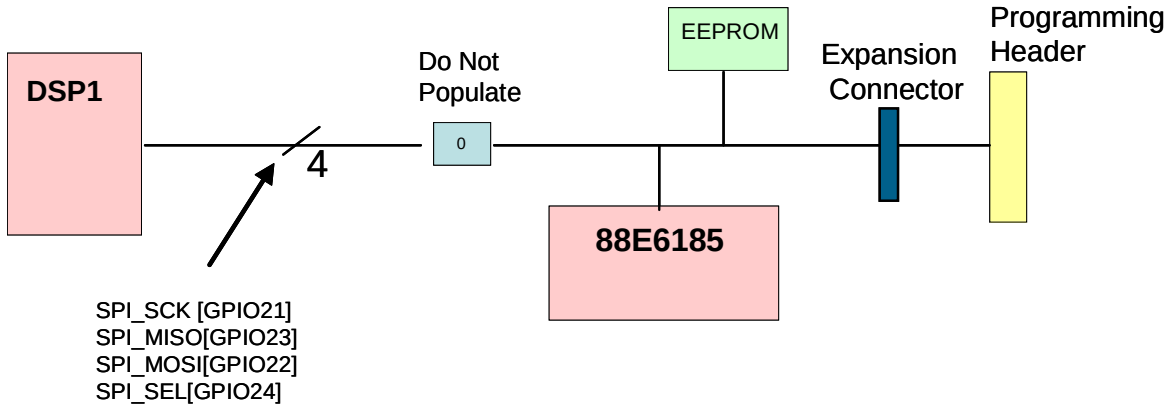


Figure 5-12. MSC8144 SPI

5.2 MSC8144 to Backplane Serial RapidIO Connectivity

The board uses a Tundra TSI578 Switch to connect the MSC8144 serial RapidIO interface to the backplane. The switch also connects to the MSC8144 I^2C bus.

5.2.1 Tundra TSI578 Serial RapidIO Switch

The TSI578 provides high-performance serial RapidIO interfaces that provide connectivity for control and data plane applications. It features eight x4 Serial Rapid IO ports running at up to 3.125 Gbps. Four of the ports are connected to the MSC8144s and four are connected to the AMC backplane. Two of these connections connect to the fat pipes section of the AMC Connector Ports[4:7] and Ports[8:11]. The final two ports connect to the “Extended Options” region Ports[12:15] and Ports[17:20]. These two are for proprietary use and are multiplexed with the TDM interface via a three pad populate/no populate zero resistor option. Table 5-13 lists the configuration settings for the TSI578.

Table 5-13. TSI578 Configuration

Signal	Description	Pin Setting	Comment
I2C_DISABLE	Disable I^2C register loading after reset	Pull Up	I^2C Loading is not required
SP_RX_SWP	Configures the order of 4x receive lanes on serial ports [0,2,4,6...14]	Pull Up (DNP)	Internal Pull down selects 0=A,B,C,D Optional pull up resistor for setting =1 [D,C,B,A] ordering

Table 5-13. TSI578 Configuration (continued)

Signal	Description	Pin Setting	Comment
SP_TX_SWP	Configures the order of 4x transmit lanes on serial ports [0,2,4,6...14]	Pull Up (DNP)	Internal Pull down selects 0=A,B,C,D Optional pull up resistor for setting =1 [D,C,B,A] ordering
SP_IO_SPEED[0:1]	Serial Port Tx/RX operating frequency 00 = 1.25Gbit/s 01 = 3.125Gbit/s (default) 10 = 2.5Gbit/s 11 = illegal	Connected to switch and system CPLD	Switch controlled
SP[1,3,5,7,9,11,13,15] PWRDN	Power down the port 0 = Powered Up 1 = Powered Down	Not connected (internal pull up)	Port powered down
SP[2,4,6,8,10,12,14] PWRDN	Power down the port 0 = Powered Up 1 = Powered Down	Pulled low	Port powered up
SP[0.2.4.6.8.10.12,14] MODE_SEL	0 = x4 mode 1 = x1 mode	Pull up (DNP)	Internal Pull down for x4. Optional pull up resistor available for up for x1 mode
MCES	Multicast Event symbol (output)	Connected to test point	Debug use
BCE	Boundary Scan Compatibility Enable	Pull Down (DNP)	Internal pull up Optional pull down to activate on-DIE scope
I2CSEL	0 = I2CSA[1:0] bits ignore, lower bits of EPROM address default to 00 1 = I2CSA[1:0] bits used as lower bits of EPROM address	Pull Down (DNP)	Option: Remove pull down for internal pull up (I2CSEL=1)
I2CSA[1:0]	LSB 2 bit so address	Pulled low	Address =0bxxxxx00. Option: Remove pull down for internal pull up (0bxxxxxxx)
I2CMA	0=single byte peripheral address 1=multi-byte peripheral address	Pulled low	Single byte selected. Remove pull down for internal resistor pull up option

There are two switches available that control the Serial Port speed of the TSI 578, shown in Table 5-14.

Table 5-14. Serial Port Speed Select

Feature	Settings [OFF=1 ON=0]	Comments
SW3.1 SW3.2	SW3.1/SW3.2 ON/ON ON/OFF OFF/ON OFF/OFF	SP_IO_SPEED[0:1]: Select TSI578 serial RapidIO clock speed 00:1.25 GHz 01: 3.125 GHz 10: 2.5 GHz 11: illegal

5.2.2 I^2C Interface

The TSI578 is connected to the MSC8144 I^2C bus via zero Ω DNP resistors to allow direct programming from DSP1.

5.3 MSC8144 to Backplane Ethernet Connectivity

The AMC board uses a Marvell 88E6185 Ethernet switch to connect the Ethernet connections to the backplane.

5.3.1 Marvell 88E6185 Ethernet Switch

The 88E6185 interfaces the backplane to the MSC8144 subsystem. Two ports from the backplane are connected to the switch. The switch then routes Ethernet traffic to the DSP Farm. In addition, the switch connects to an Ethernet debug port via the expansion connector.

5.3.2 Marvell 88E6185 Ethernet Switch Configuration

Table 5-15 summarizes the port allocation and physical interconnect interface on the 88E6185.

Table 5-15. Ethernet Switch Ports

88E6185 Port	Interconnect Interface	Target	Description
0	SGMII	DSP1	via the 88E1145
1	SGMII	DSP2	via the 88E1145
2	SGMII	DSP3	via the 88E1145
3	SGMII	DSP4	via the 88E1145
4	—	—	—
5	—	—	—
6	SGMII	88E1111 Eth PHY	PHY/RJ45
7	1000BASE-X	AMC Connector Port 0	GigE Control
8	1000BASE-X	AMC Connector Port 1	GigE Control
9	—	—	—

Table 5-16. 88E6185 Switch Configuration Settings

88E6185 Signal	Pin Setting	Description
EE_1K	Pull Down (DNP)	Internal Pull Up = 16-Bit Addressing for EEPROM
FD_FLOW_DS	Pull Down	Enables Flow Control on Full Duplex Ports
HD_FLOW_DS	Pull Down	Enable Flow Control on Half Duplex Ports
PPU_EN	Pull Up	Enable the PHY Polling Unit
SW_MODE0	Pull Down (DNP)	Internal pull up => SW[MODE[1:0] = 11; EPROM Attached Mode
SW_MODE1	Pull Down (DNP)	
ADDR0[4:0]	10000	SMI Address = 0x10
MGMII	Low	SerDes PHY Interface
P7_MODE	High	Port 7 Configured for 1000 Base-X
P8_MODE	High	Port 8 Configured for 1000 Base-X
P9_MODE[2:0]	111	Port 9 disabled, pins tri-state
CONTROL	n/c	Controls a PNP for 1.2 V generation (not used)

The default configuration of the 88E6185 does not support SGMII on ports 0–3 and 6, so programming of certain registers is required after reset. The programming of these registers is done via the external EEPROM, which is read after reset is released.

5.3.3 Marvell 88E1145 Quad PHY

The 88E1145 is the interface between the MSC8144 RGMII and the SGMII Ethernet switch. Each port operates in an identical manner performing RGMII to SGMII conversion. Port configuration is via configuration pins and a serial management interface.

5.3.4 Marvell 88E1145 Configuration

The PHY is reset from the Reset CPLD during power up via the CPLD signal QPHY_RESET_N. Each of the four ports has an interrupt that is fed back to the MSC8144 via the system logic CPLD. The polarity of this interrupt is programmable. The 88E1145 register block can be programmed via the management interface, with each port connected to its associated MSC8144 MDIO/MDC interface. The configuration of Ports 0–3 of the 88E1145 PHY is detailed in Table 5-17.

Table 5-17. Ethernet Port Configuration

Port 0 Config [DSP1]	Bit	Description
CONFIG 0	0000	Address = 0x0
CONFIG 1	0110	RGMII to SGMII Conversion
CONFIG 2	1111	Auto negotiate, Advertise capabilities, Prefer Slave
CONFIG 3	0101	Address MSB=0; Enable cross-over, Enable Detect; Dis. Energy
CONFIG 4	0000	Enable MDIO, Enable Pause
Port 1 Config [DSP2]	**Bit**	**Description**
CONFIG 0	0001	Address = 0x1
CONFIG 1	0110	RGMII to SGMII Conversion
CONFIG 2	1111	Auto negotiate, Advertise capabilities, Prefer Slave
CONFIG 3	0101	Address MSB=0; Enable cross-over, Enable Detect; Dis. Energy
CONFIG4	0000	Enable MDIO, Enable Pause
Port 2 Config [DSP 3]	**Bit**	**Description**
CONFIG 0	0010	Address = 0x2
CONFIG 1	0110	RGMII to SGMII Conversion
CONFIG 2	1111	Auto negotiate, Advertise capabilities, Prefer Slave
CONFIG 3	0101	Address MSB=0; Enable cross-over, Enable Detect; Dis. Energy
CONFIG 4	0000	Enable MDIO, Enable Pause
Port 3 Config [DSP 4]	**Bit**	**Description**
CONFIG0	0011	Address = 0x3
CONFIG 1	0110	RGMII to SGMII Conversion
CONFIG 2	1111	Auto negotiate, Advertise capabilities, Prefer Slave
CONFIG 3	0101	Address MSB=0; Enable cross-over, Enable Detect; Dis. Energy
CONFIG 4	0000	Enable MDIO, Enable Pause
Global Configuration	**Bit**	**Description**
GCONFIG0	0000	Enable DTE Detect, 50ohm termination, 4 MDIO ports, Enable 125 MHz Clock
GCONFIG1	0111	LED Blink, SD pins not used for signal detect, Active low interrupt

5.3.5 Marvell 88E1111 Ethernet PHY Configuration

The Marvell 88E1111 Gigabit PHY is used to terminate the Gigabyte Ethernet frontplane traffic via the expansion connector. The PHY is configured at Reset via its CONFIG[6:0] pins. These pins are tied to ground, V_{CC}, or one of the LED pins to give the bit settings described in Table 5-18.

Table 5-18. 88E1111 Pin to Constant Encoding

Pin	Bit[2:0]
VCC	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GROUND	000

The PHY on the MSC8144AMC-S is configured as shown in Table 5-19 and Table 5-20.

Table 5-19. 88E1111 PHY Configuration Settings

Pin	Bit[2]	Bit[1]	Bit[0]	Encoding	Hardware Connection
CONFIG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	110	LED_LINK10
CONFIG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	VSS
CONFIG2	ANEG[3]	ANEG[2]	ANEG[1]	110	LED_LINK10
CONFIG3	ANEG[0]	ENA_XC	DIS_125	011	LED_RX
CONFIG4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]	100	LED_LINK1000
CONFIG5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]	110	LED_LINK10
CONFIG6	SEL_TWSI	INT_POL	75/50 OHM	010	VSS

Table 5-20. 88E1111 PHY Configuration Description

Configuration	Value	Description
PHYADR[4:0]	0x00110	PHY is on Ethernet Switch Port 6 (0x00110)
ENA_PAUSE	0	Default register 4.11:10 to 00 - copper
ANEG[3:0]	0x1100	Auto-Negotiation for Copper Modes 1100 = Auto-Neg, advertise all capabilities, forced Master
ENA_XC	1	Enable Crossover.
DIS_125	1	Disable 125 CLK
HWCFGMODE[3:0]	0100	Hardware configuration mode: SGMII without Clock with SGMII Auto-Neg to Copper
DIS_FC	1	Disable fibre (SERDES)/copper auto selection
DIS_SLEEP	1	Disable energy detect
SEL_TWSI	0	Select MDC/MDIO interface
INT_POL	1	Interrupt signal is active low
75/50 OHM	0	50 ohm termination for Fibre (SERDES)

5.4 Backplane Connector

The connector provides connectivity to conductive traces on both sides of the AMC PCB. There are 170 traces in total. The connector interfaces to the following:

- Four 4x serial RapidIO interface (16 wire)
- Two Gigabyte Fiber interface for control/data
- AMC clocks
- Propriety TDM Interface
- The card is mechanically designed to fit into an AMC slot via its P1 connector. The connector is hard gold plated for improved insertion durability.

This connector pin out is described in Table 5-21.

Table 5-21. AMC Connector Site Pin Definitions [Serial RapidIO Version]

Pin #	AMC Definition	Specific Signal Description	Pin #	AMC Definition	Specific Signal Description
01	GND	—	170	GND	—
02	+12V	—	169	TDI	AMC_TDI
03	PS1#	PS1_N	168	TDO	AMC_TDO
04	MP	IPMCV	167	TRST#	AMC_TRST
05	GA0	GA0	166	TMS	AMC_TMS
06	RSRVD	n/c	165	TCLK	AMC_TCLK
07	GND	—	164	GND	—
08	RSRVD	n/c	163	TX20+	AMC4_SrRIO_TXD_P3
09	+12V	—	162	TX20-	AMC4_SrRIO_TXD_N3
10	GND	—	161	GND	—
11	TX0+	AMC_TXD_P0_P	160	RX20+	AMC4_SrRIO_RXD_P3
12	TX0-	AMC_TXD_P0_N	159	RX20-	AMC4_SrRIO_RXD_N3
13	GND	—	158	GND	—
14	RX0+	AMC_RXD_P0_P	157	TX19+	AMC4_SrRIO_TXD_P2
15	RX0-	AMC_RXD_P0_N	156	TX19-	AMC4_SrRIO_TXD_N2
16	GND	—	155	GND	—
17	GA1	GA1	154	RX19+	AMC4_SrRIO_RXD_P2
18	+12V	—	155	RX19-	AMC4_SrRIO_RXD_N2
19	GND	—	152	GND	—
20	TX1+	AMC_TXD_P0_P	151	TX18+	AMC4_SrRIO_TXD_P1
21	TX1-	AMC_TXD_P0_N	150	TX18-	AMC4_SrRIO_TXD_N1
22	GND	—	149	GND	—
23	RX1+	AMC_RXD_P0_P	151	RX18+	AMC4_SrRIO_RXD_P1
24	RX1-	AMC_RXD_P0_N	150	RX18-	AMC4_SrRIO_RXD_N1
25	GND	—	146	GND	—
26	GA2	GA2	145	TX17+	AMC4_SrRIO_TXD_P0
27	+12V	—	144	TX17-	AMC4_SrRIO_TXD_N0
28	GND	—	143	GND	—
29	TX2+	n/c	142	RX17+	AMC4_SrRIO_RXD_P0
30	TX2-	n/c	141	RX17-	AMC4_SrRIO_RXD_N0
31	GND	—	140	GND	—

Table 5-21. AMC Connector Site Pin Definitions [Serial RapidIO Version] (continued)

Pin #	AMC Definition	Specific Signal Description	Pin #	AMC Definition	Specific Signal Description
32	RX2+	n/c	139	TCLKD+	TCLKD_P
33	RX2-	n/c	138	TCLKD-	TCLKD_N
34	GND	—	137	GND	—
35	TX3+	n/c	136	TCLKC+	TCLKC_P
36	TX3-	n/c	135	TCLKC-	TCLKC_N
37	GND	—	134	GND	—
38	RX3+	n/c	133	TX15+	AMC3_SrRIO_TXD_P3
39	RX3-	n/c	132	TX15-	AMC3_SrRIO_TXD_N3
40	GND	—	131	GND	—
41	ENABLE #	ENABLE_N	130	RX15+	AMC3_SrRIO_RXD_P3
42	+12V	—	129	RX15-	AMC3_SrRIO_RXD_N3
43	GND	—	128	GND	—
44	TX4+	AMC1_sRIO_TXD_P0	127	TX14+	AMC3_SrRIO_TXD_P2
45	TX4-	AMC1_sRIO_TXD_N0	126	TX14-	AMC3_SrRIO_TXD_N2
46	GND	—	125	GND	—
47	RX4+	AMC1_sRIO_RXD_P0	124	RX14+	AMC3_SrRIO_RXD_P2
48	RX4-	AMC1_sRIO_RXD_N0	123	RX14-	AMC3_SrRIO_RXD_N2
49	GND	—	122	GND	—
50	TX5+	AMC1_sRIO_TXD_P1	121	TX13+	AMC3_SrRIO_TXD_P1
51	TX5-	AMC1_sRIO_TXD_N1	120	TX13-	AMC3_SrRIO_TXD_N1
52	GND	—	119	GND	—
53	RX5+	AMC1_sRIO_RXD_P1	118	RX13+	AMC3_SrRIO_RXD_P1
54	RX5-	AMC1_sRIO_RXD_N1	119	RX13-	AMC3_SrRIO_RXD_N1
55	GND	—	116	GND	—
56	SCL_L	AMC_SCL	115	TX12+	AMC3_SrRIO_TXD_P0
57	+12V	—	114	TX12-	AMC3_SrRIO_TXD_N0
58	GND	—	113	GND	—
59	TX6+	AMC1_sRIO_TXD_P2	112	RX12+	AMC3_SrRIO_RXD_P0
60	TX6-	AMC1_sRIO_TXD_N2	111	RX12-	AMC3_SrRIO_RXD_N0
61	GND	—	110	GND	—
62	RX6+	AMC1_sRIO_RXD_P2	109	TX11+	AMC2_SrRIO_TXD_P3
63	RX6-	AMC1_sRIO_RXD_N2	108	TX11-	AMC2_SrRIO_TXD_N3
64	GND	—	107	GND	—
65	TX7+	AMC1_sRIO_TXD_P3	106	RX11+	AMC2_SrRIO_RXD_P3
66	TX7-	AMC1_sRIO_TXD_N3	105	RX11-	AMC2_SrRIO_RXD_N3
67	GND	—	104	GND	—
68	RX7+	AMC1_sRIO_RXD_P3	103	TX10+	AMC2_SrRIO_TXD_P2
69	RX7-	AMC1_sRIO_RXD_N3	102	TX10-	AMC2_SrRIO_TXD_N2
70	GND	—	101	GND	—
71	SDA_L	AMC_SDA	100	RX10+	AMC2_SrRIO_RXD_P2
72	+12V	—	99	RX10-	AMC2_SrRIO_RXD_N2
73	GND	—	98	GND	—
74	CLKA+	TCLKA_P	97	TX9+	AMC2_SrRIO_TXD_P1
75	CLKA-	TCLKA_N	96	TX9-	AMC2_SrRIO_TXD_N1
76	GND	—	95	GND	—

Table 5-21. AMC Connector Site Pin Definitions [Serial RapidIO Version] (continued)

Pin #	AMC Definition	Specific Signal Description	Pin #	AMC Definition	Specific Signal Description
77	CLKB+	TCLKB_P	94	RX9+	AMC2_SrRIO_RXD_P1
78	CLKB-	TCLKB_N	93	RX9-	AMC2_SrRIO_RXD_N1
79	GND	—	92	GND	—
80	FCLKA+	NC	91	TX8+	AMC2_SrRIO_TXD_P0
81	FCLKA-	NC	92	TX8-	AMC2_SrRIO_TXD_N0
82	GND	—	89	GND	—
83	PS0#	PS0_N	88	RX8+	AMC2_SrRIO_RXD_P0
84	+12V	—	87	RX8-	AMC2_SrRIO_RXD_N0
85	GND	—	86	GND	—

The serial RapidIO x4 pipes that connect to the extended options region (Ports12–20) are multiplexed with the TDM interface. The layout/routing is designed to maintain the desired levels of signal integrity on the SIO signals.

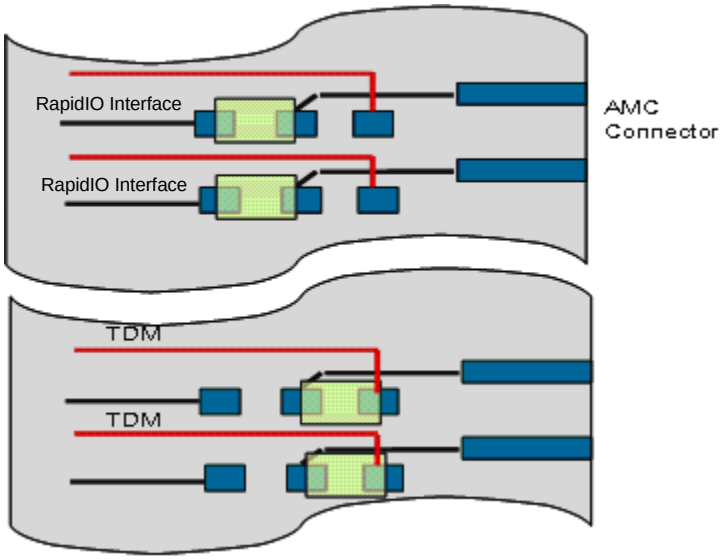


Figure 5-13. Serial RapidIO/TDM Signal Multiplexing

5.5 General Board Configuration

The following subsections described general board configuration issues.

5.5.1 Reset Operation and Connectivity

Reset control of the board is provided by the Reset CPLD. It provides the following functions:

- Power Control
- Reset Control
- JTAG routing (non-MSC8144)

The CPLD is powered from IPMCV 3.3 V and can work stand-alone or in conjunction with the MMC to power up and control the board. When in a chassis, the CPLD receives control signals from the AMC backplane and powers up the board. When in standalone mode (switch selectable). The CPLD waits for the detection of a 12 V signal and then powers up the board via the CPLD Power Sequencer. Details can be found in Section 5.5.2, "System CPLD" and Section 5.7, "Module Management Controller (MMC)."

The CPLD Reset Sequencer is used to control the reset of all devices on the board. To facilitate BSCAN testing of all the Ethernet and serial RapidIO components, their JTAG signals have been routed to the CPLD for use by the BSCAN tester, shown in Figure 5-20.

A 66 MHz clock oscillator is used to internally clock the device. This is connected to the general purpose clock pin, GCLK0.

There are two reset CPLD DIP switches that provide the configuration shown in Table 5-22.

Table 5-22. Reset CPLD Switches

Feature	Settings [OFF=1 ON=0]	Comments
SW3.3	ON OFF	Reset CPLD controlled Power Up ColdFire controlled MMC
SW3.4	ON	Future use

There are two status LEDs that provide the information shown in Table 5-23.

Table 5-23. Reset CPLD LEDs

Feature	Color	Comments
LD602	Yellow	ON-3.3 V present OFF 3.3 V not present
LD601	Green	ON-Power Good OFF Power Fail

5.5.1.1 Reset Control

The reset scheme is shown in Figure 5-14. The CPLD controls the reset to all the devices. A single reset controls the Ethernet Quad PHY (88E1145) and Single PHY (88E1111). For the Ethernet switch (88E6185) a single reset from the CPLD is combined with a reset from the EPROM programmer for reset control. The CPLD produces two resets for the TSI578, the Hard Reset (SRIO_RESET_N) and the Soft Reset (SW_RESET_N).

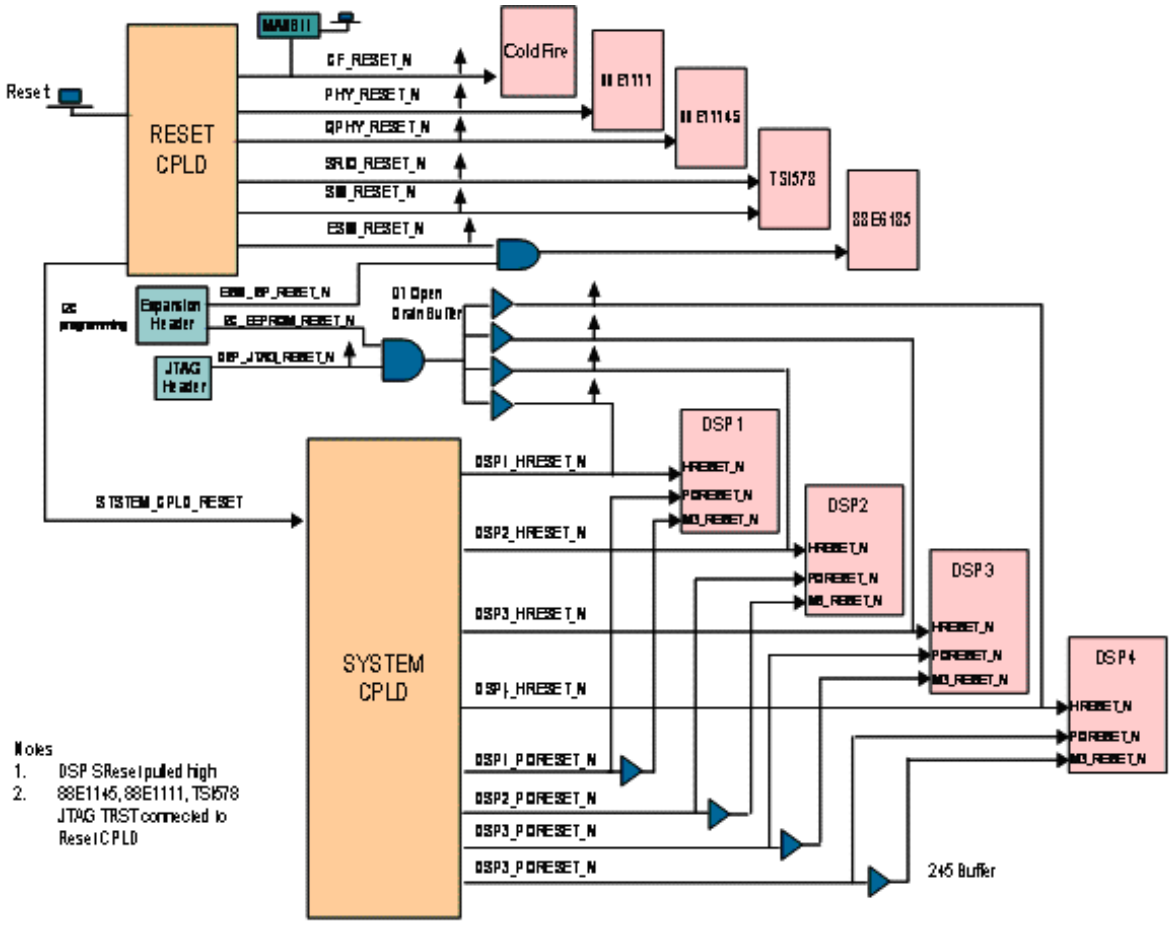


Figure 5-14. Reset Scheme

The JTAG resets for the 88E1111, 88E1145 and TSI578 are routed from the CPLD so the CPLD can control both JTAG and device reset. The MSC8144 has three external reset sources, Power on Reset ($\overline{\text{PORESET}}$), Hard Reset ($\overline{\text{HRESET}}$), and Soft Reset ($\overline{\text{SRESET}}$). The soft reset is not used in the system and is pulled high. The DSP sub-system reset is controlled from the Reset CPLD via the signal SYSTEM_RESET_CPLD. This signal controls the reset sequencer in the System CPLD. The System CPLD controls the $\overline{\text{PORESET}}$, $\overline{\text{M3\_RESET}}$ and $\overline{\text{HRESET}}$ of the four MSC8144s. The SRESET signals for the MSC8144s are pulled high. To facilitate I^2C programming, the programmer reset signal from the expansion connector is combined with the DSP $\overline{\text{HRESET}}$ signal. Note that the M3 reset is not 3.3 V-tolerant, which is why the board includes the level shifter logic for 2.5 V.

5.5.2 System CPLD

The system CPLD provides the following functionality:

- Interfaces MSC8144 TDM to the AMC backplane connector
- Drives the reset and configuration for the MSC8144
- Collect and distribute the GPIO/Interrupts on the board
- Multiplexes MSC8144 UARTs and routes a single UART to the expansion connector

There are six System CPLD DIP switches described in Table 5-24 and Table 5-25.

Table 5-24. System CPLD Switches

Feature	Settings [OFF=1 ON=0]	Comments
SW3.1	ON	Not used in CPLD. Switches connect directly to TSI578 to control serial RapidIO frequency.
SW3.2	OFF	

Table 5-25. System CPLD Switches

Feature	Settings [OFF=1 ON=0]	Comments
SW4.1 SW4.2	SW4.1/SW4.2 ON/ON ON/OFF OFF/ON OFF/OFF	Select MSC8144 UART output 00 – DSP1 01 – DSP2 10 – DSP3 11 – DSP4
SW4.3	ON OFF	Reset Configuration Word from I^2C, Boot port = serial RapidIO interface Reset Configuration Word from pins, Boot Port = I^2C
SW4.4	ON OFF	Debug OFF [EE0=0] Debug ON [EE0=1]

There are also two status LEDs, which provide the information shown in Table 5-26.

Table 5-26. Reset CPLD LEDs

Feature	Color	Comments
LD612	Yellow	MSC8144 HRESET (Logical AND of all DSP HRESET signals)
LD609	Green	MSC8144 PORESET (Logical AND of all DSP PORESET signals)

5.6 Power Supply

There are two separate power rails inputs to the card, as follows:

- 3.3 V Management Power (IPMCV)— used to power MMC circuitry
- 12 V Payload Power—used to power the rest of the board

All of the required voltages for the card are generated locally on board from the 12 V supply using DC-DC converters.

5.6.1 Power Requirements

The MSC8144AMC-S has a number of on-board peripheral chips, each with its own voltage and power requirements. Table 5-27 highlights the main peripheral chips used on the MSC8144AMC-S and their individual voltage/power requirements.

Table 5-27. Estimated Board Power Requirements

Device	Power (W)	Comments
MSC8144	Application dependent	Contact Freescale
TSI578	3.6 W	—
88E1145	0.57 W	—
88E6185	1.5 W	—
88E1111	1.0 W	—
MT47H64M16	0.5 W x 8 = 4 W	—
EPM240T1005CN	0.2 W	Estimated
EPM1270F256C3N	0.2 W	Estimated
MCF5213	0.05 W	—
DS90LV049	0.07 W	—
DS90LV028A	0.018 W	—
ICS8543	0.165 W	—
ICS9112	0.1 W	—

There are a number of devices that have voltage rail, ramp up dependencies, described as follows:

- The Ethernet switch can power up in two ways, as follows:
  - — All voltages at the same time
  - — Highest to lowest (3.3 V, 2.5 V, 1.5 V, 1.2 V)
- The TSI should be powers up with 1.2 V first followed by 3.3 V
- The MSC8144 powers up with 1.0 V first followed by 3.3 V

5.6.2 Power Supply Operation

To accommodate all the various power up requirements, use the power scheme shown in Figure 5-15 with all timing controlled by the Reset CPLD.

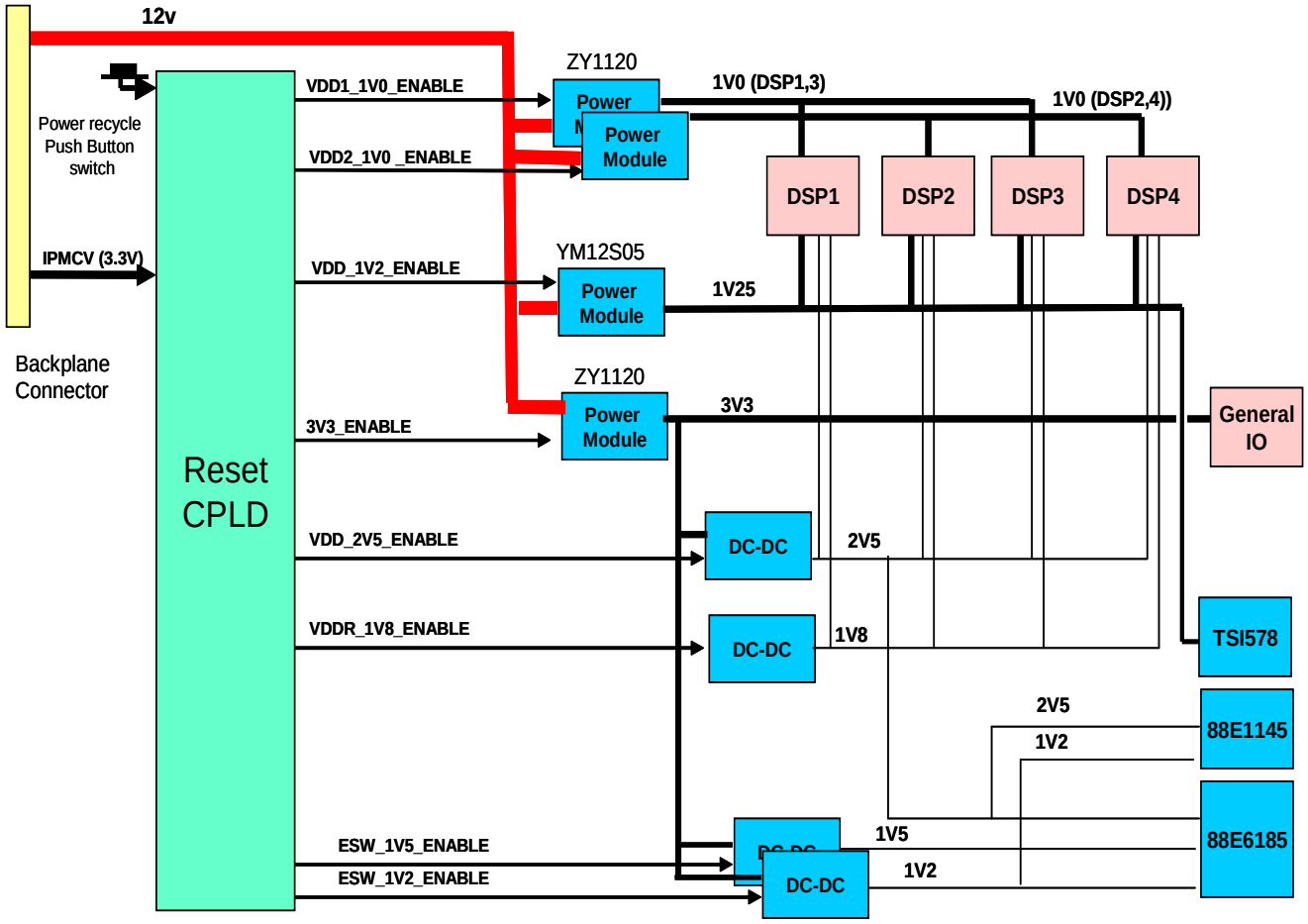


Figure 5-15. Power Distribution

The board receives IPMCV (3.3 V), 12 V, and ground from the AMC edge connector (or 3-pin terminal for standalone operation). The 12 V is fed to four DC-DC power modules. Two vertical “Power One ZY1120” 20 A capable modules are used to generate the DSP Core voltages (two DSPs per module). A third ZY1120 is used to generate the 3.3 V. A fourth Power One YM12S05 5A module supplies power to the 1.25 V rail. This supplies the TSI578 and the MSC8144 M3 memory.

The 3.3 V is also used to generate a number of the peripheral voltages. These include 2.5 V (M3), 1.8 V (DDR2), 1.5 V, and 1.2 V (both Ethernet switches).

NOTE

The different power sequencing requirements of the TSI578 and the 88E6185 require separate core supplies.

The output voltage of the ZY1120 power modules is defined by the following equation:

$$Rtrim = \frac{20 \times (5.5 - Vout)}{Vout}$$

An 88.7 KΩ trim resistor is used for 1.0 V and a 13 KΩ is used for 3.3 V.

The output voltage of the YM12S05 is set using the following equation:

$$Rtrim = \frac{20.5}{(Vout - 0.7525)} - 1$$

A 22.45 KΩ trim resistor gives the required 1.25 V. This is provided via two 40.2 KΩ resistors in parallel for enhanced stability.

Two “Maxim MAX8869” 1 A DC-to-DC converters are used to generate the Ethernet Switch 1.5 V and 1.2 V voltages (ESW_1V5 and ESW_1V2). A third MAX8869 is used to generate the M3 2.5 voltage. The output voltage of the MAX8869 is set using the following equation:

$$Vout = 0.8\left(1 + \frac{R1}{R2}\right)$$

Where Rout connects the SET pin to Vout and R2 connects the SET pin to ground.

For 1.5 V, R1 = 10 KΩ and R2 = 11.3 KΩ

For 1.2 V, R1 = 10 KΩ and R2 = 20 KΩ

For 2.5 V, R1 = 10 KΩ and R2 = 4.7 KΩ

The 1.8 V DDR voltage is supplied by a 4 A Maxim MAX8556 DC-to-DC converter. The output voltage is set using the following equation:

$$R2 = R3\left(\frac{Vout}{0.5} - 1\right)$$

Where R2 connects the FB pin to Vout and R3 connects the FB pin to ground.

For 1.8 V, R2 = 2.6 KΩ, and R3 = 1 KΩ

All the DC to DC converters are controlled by the Reset CPLD. The CPLD controls the ENABLE signals to bring the power up in a controlled manner as required by the various device specifications. In turn, the POWER GOOD signals are fed back from the various devices to the Reset CPLD to enable it to manage the power up process. The power-up sequence is as follows:

1. MSC8144 Core Voltages (1.0 V)
2. TSI578, M3 Core voltages (1.25 V)
3. I/O voltage (3.3 V)
4. Ethernet Switch IO voltage and M3 voltage (2.5 V)
5. DDR (1.8 V)
6. Ethernet Switch IO voltage (1.5 V)
7. Ethernet Switch Core voltage (1.2 V)

This power up procedure satisfies the main sequencing requirements, which are that the MSC8144 and TSI578 Core voltages should be up before the 3.3 V. It also meets the reverse requirement for the Ethernet switch, which is that the 3.3 V I/O voltage should be up before its 1.25 V Core voltage.

5.7 Module Management Controller (MMC)

The MSC8144AMC-S incorporates a module management controller, which resides on the on-board ColdFire® device. The MMC software is supplied by CorEdge and is programmed into the Coldfire device internal Flash. The MMC provides the following functions:

- Module Hot Swap manger to facilitate AMC insertion and extraction.
- Monitors and controls power using the voltage sensors and power switches.
- Monitors temperature using 2 temperature sensors.
- Monitors faults and reset MMC in event of fault using MMC Watch dog timer (WDT).
- Provides Flash memory for FRU records.
- Provides visible module status information using the mandatory blue LED (hot swap state) and red LED (fault condition).

5.7.1 MMC Implementation

The MMC uses a 32-bit MCF5213 ColdFire microcontroller that communicates with the intelligent platform management controller (IPMC) on the carrier card or µTCA Carrier Hub (MCH) in a µTCA system, over the intelligent platform management bus (IPMB), as shown in Figure 5-16.

The MMC uses the signal CF_ENABLE_PWR to control the power and reset sequence generators in the Reset CPLD (see Figure 5-17). In addition the AMC was designed so that in environments in which the MMC is not present, the Reset CPLD can power up the board in standalone mode (switch selectable using SW3.3). The Coldfire device supports a UART port and a Background Debug Module (BDM) via the expansion connector.

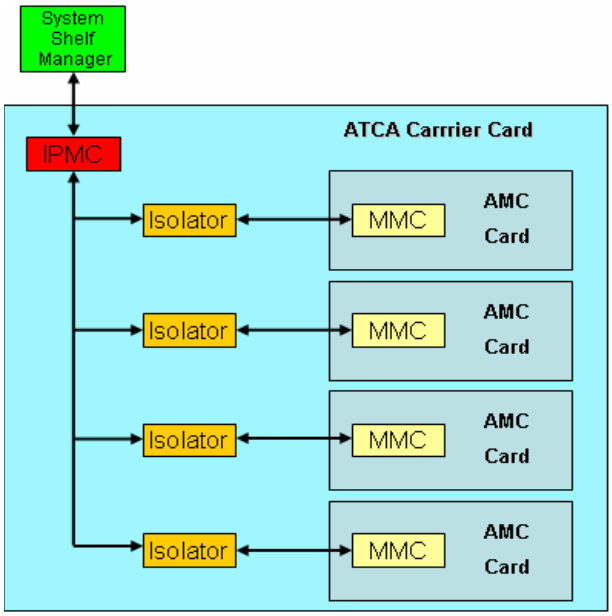


Figure 5-16. IPMC/IPMB Module Management

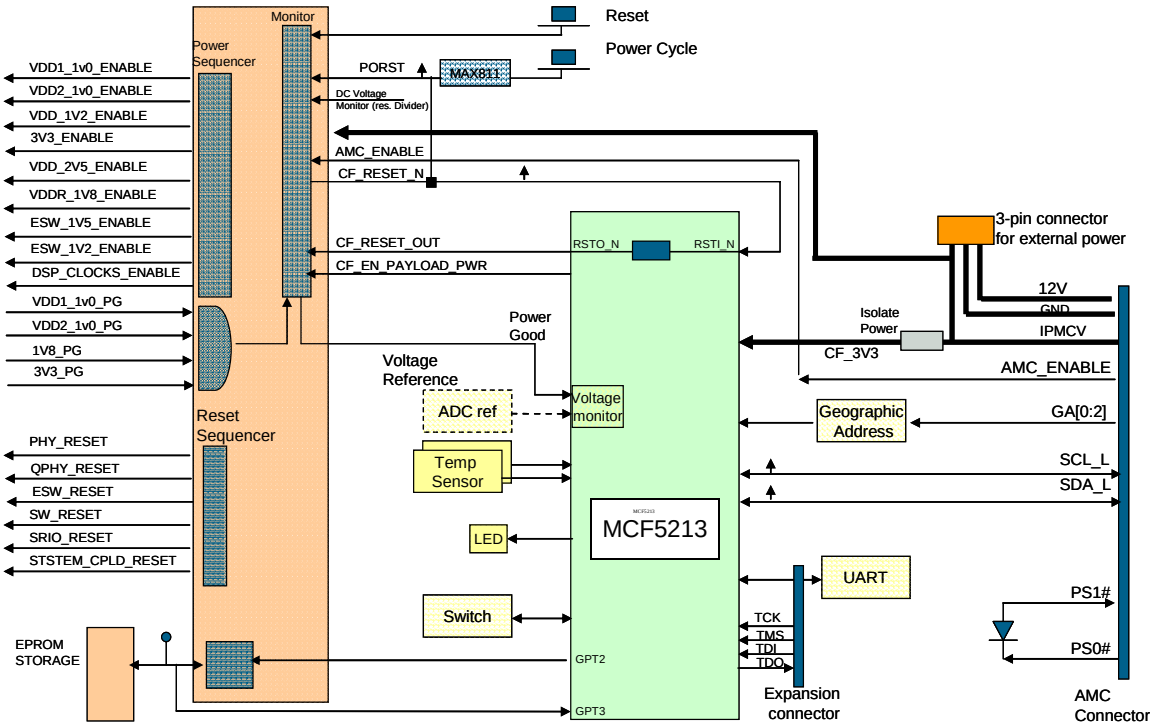


Figure 5-17. MMC/Reset CPLD Implementation

5.7.2 MMC Operation Overview

The following subsections give a general overview of MMC operation.

5.7.2.1 Module Insertion

Last mate pins PS0_N and PS1_N are used to indicate that the module is inserted. The PS1_N is pulled high by the IPMC (either by ATCA carrier or MicroTCA MCH). The module when fully inserted pulls PS1_N to module ground via a diode. PS1_N going low indicates the module presence to the IPMC. The IPMC senses low signal on PS1 and supplies Management Power (MP). The MP (IPMCV) is 3.3 V and cannot draw more than the AMC.0 specified 150 mA limit.

5.7.2.2 Enabling the MMC

Upon insertion, the MMC powers up and is held in a reset state until the AMC_ENABLE_N signal is pulled low. The carrier IPMC releases the module from this state by driving the AMC_ENABLE_N signal high. This is routed through the Reset CPLD to the Coldfire via the signal CF_RESET_N.

5.7.2.3 Status LEDs

Two LEDs for system status are mandated by the AMC.0 specification. These are the Blue LED and Red LED. The Red LED switches on to indicate a fault condition. The IPMC drives the state of the Blue LED during power up/hot swap operations. Figure 5-18 details the states.

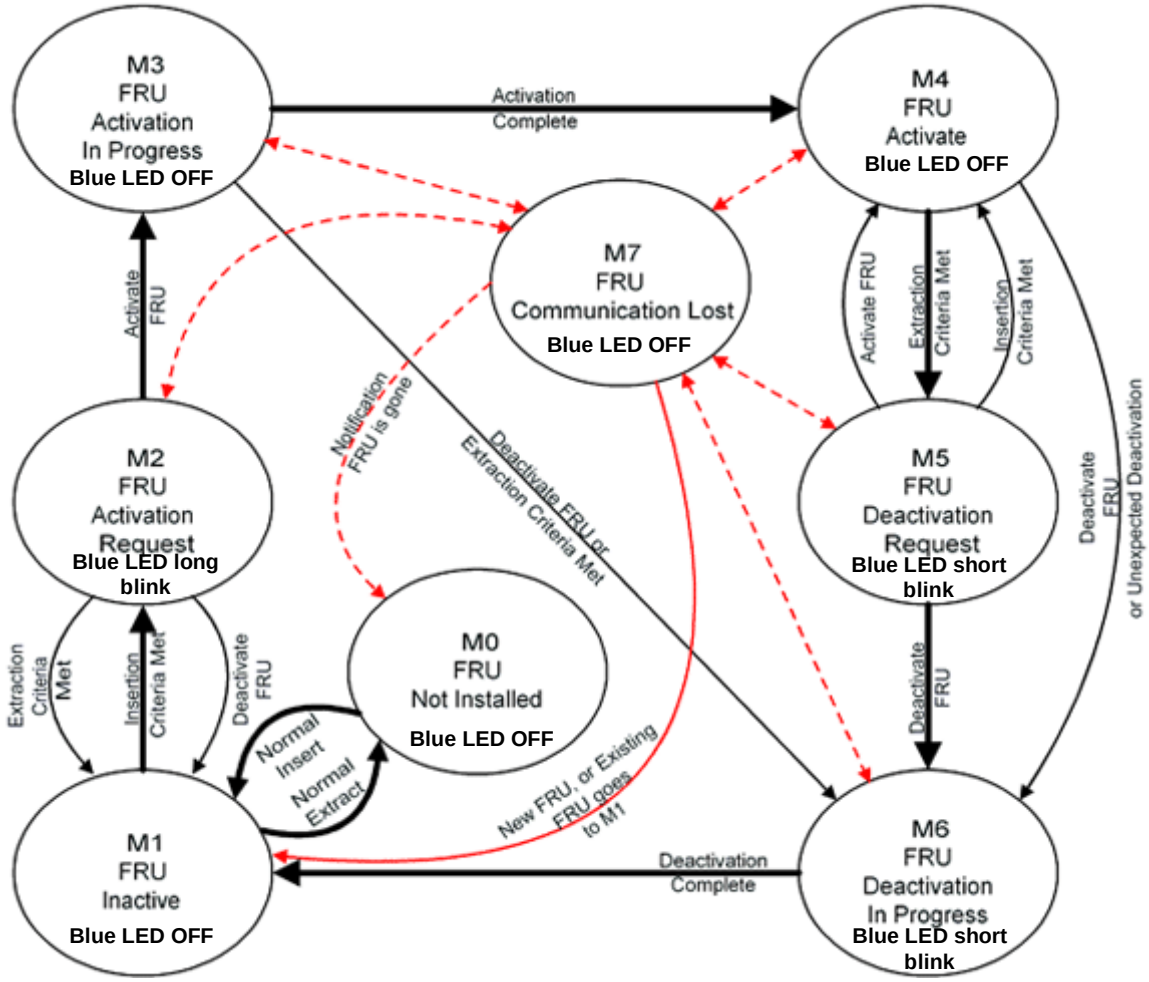


Figure 5-18. FRU State Transition Diagram

5.7.2.4 Hot Swap Switch

The Hot Swap Switch is activated by the Module latching mechanism and is used to confirm insertion or indicate a request for an extraction to the MMC. This switch signal is pulled up to Management Power so that it can be read when Payload Power is not applied. The MMC sends an event to the Carrier IPMC when the Hot Swap Switch changes state.

5.7.2.5 Module Management Communications Bus (IPMB-L)

Out Of Band (OOB) module management may be facilitated by utilizing messages carried over IPMB-L. The IPMB-L is an I^2C bus with clock line AMC_SCL and data line AMC_SDA.

5.7.2.6 Geographical Address (GA[2:0])

Three Geographic Address (AMC_GA[0:2]) pins represent the module address to the IPMC. Each GA line is in one of 3 states: High, Ground or Unconnected. The MMC senses the logical states of these pins to determine its unique IPMB-L address.

5.7.2.7 Module temperature Sensors

The MMC supports two temperature sensors. The MMC monitors the temperature sensors and this data can be identified in the MMC Sensor Data Records

5.7.2.8 Module Voltage Sensors

Voltage sensors report the status of the power within the module. The MMC supports 5 power sources:

- 12 V
- 3.3 V
- 2.5 V
- 1.8 V
- 1.5 V

5.7.2.9 MMC UART

The MMC can be interrogated by the user via the ColdFire UART connector, which is located on the expansion card.

5.7.2.10 BDM Debug Header

The ColdFire device can be programmed via the BDM header, which is located on the expansion header.

5.7.2.11 Persistent Store

The module contains a serial EEPROM (SEEPROM) which can be used to store relevant data about the AMC (Serial number, and so on). The FRU data is stored in the Coldfire device internal memory

5.7.3 MMC User Operation

The following sections describe how to use the MMC functionality.

5.7.3.1 Hot-Swapping

To hot-swap a board, complete the steps listed in the following sections.

5.7.3.1.1 Hot-Swapping a Board In

Use the following steps to install the board when hot-swapping:

1. Set switch SW4.3 to OFF to select the MMC option.
2. Insert the AMC board with the handle extracted into an empty slot in the chassis. The BLUE LED switches ON once the board is inserted. The 3.3 V (IPMCV) also switches on
3. Close the handle. The BLUE LED flashes and then switches OFF. The board powers up in the following standard LED sequence.
   a) The 3.3V (IPMCV) stays ON.
   b) The Power Good lights and stays ON.
   c) The four MSC8144 RGMII activity LEDs switch ON and then OFF.
   d) Ethernet port activity LEDs switch ON to indicate any Ethernet link to the backplane (system-dependent).
   e) The DSP HRESET and PORESET LEDs switch ON and then OFF to indicate the reset sequence is complete.

5.7.3.1.2 Hot-Swapping a Board Out

Use the following steps to remove the board when hot-swapping:

1. Extract the hot swap handle.
2. The BLUE LED flashes and then stay ON. All LEDs except the 3.3 V (IPMCV) switch OFF.
3. When the BLUE LED is ON, the AMC can be removed from the chassis.

5.7.3.2 UART Terminal

The MMC output can be viewed through the UART terminal of the Coldfire device (via the expansion card). The UART operates at 19200 -8-N-1 terminal setting. The output is displayed in Figure 5-19.

```
*************  Port Card Management SW  *************
           Nov  9 2007,15:35:37
               40-000048-000

P: Enable dc Power           D: Disable dc Power
V: Read Voltages             T: Read Temperatures
N: Read DS2431P              E: Write DS2431P
M: Write DS2431P Test        Z: Read Card Status
K: Disable WD Pulse (Reset)  B: Turn OFF WD
C: Turn ON WD                2: Toggle Red led
3: Toggle Blue led
->
```

Figure 5-19. FRU State Transition Diagram

5.7.3.3 FRU records

The MMC contains FRU information that describes the board capabilities (e-keying and power) and inventory data. The records are described in Table 5-28 through Table 5-32.

Table 5-28. FRU Common Header

Length	Field	Value	Description
1	Common Header Format Version	01	fixed value
1	Internal Use Area Starting Offset - Multiple of 8 bytes, 00 = not present	00	Internal Use Area not present
1	Chassis Use Area starting Offset - Multiple of 8 bytes, 00 = not present	00	Chassis Use Area not present
1	Board Area starting Offset - Multiple of 8 bytes, 00 = not present	01	Board Area present, offset = 8 bytes
1	Product Info Area starting Offset - Multiple of 8 bytes, 00= not present	09	Product Info Area present, offset =64bytes
1	Multi-record Area starting Offset - Multiple of 8 bytes, 00= not present	11	Multi-record Area present, offset =128 bytes
1	PAD –fixed to 00	00	00
1	Common header Checksum	E4	

Table 5-29. FRU Board Information Area

Length	Field	Value	Description
1	Board Area Format version –	01	Fixed
1	Board Area length	08	Length =56 Bytes
1	Language Code	19	English
3	Mfg. Date / Time Number of mins from 1/1/96 - little endian	40D562	
1	**Board Manufacturer** type/length	C9	8-bit ASCII, Length= 9 Bytes

Table 5-29. FRU Board Information Area (continued)

Length	Field	Value	Description
P	Board Manufacturer bytes	46726565 7363616c 65	Freescale
1	**Board Product Name** type/length byte	CC	8-bit ASCII, Length= 12 Bytes
Q	Board Product Name bytes	4D504338 31343441 4D432D53	MPC8144AMC-S
1	**Board Serial Number** type/length byte	C5	8-bit ASCII, Length= 5 Bytes
N	Board Serial Number bytes	30303030 30	00000
1	**Board Part Number** type/length byte	C9	8-bit ASCII, Length= 9 Bytes
M	Board Part Number Bytes	3730302D 32323534 39	700-22549
13	**FRU File ID** type/length/bytes	CD	File ID
R	FRU File ID Bytes	34302D 30303030 34382D30 3031	40-000048-001
xx	Additional Custom mfg info fields	Not required	Not required
1	C1 type/length/byte encoded to indicate no more fields	C1	fixed
Y	00 - any remaining unused space	00 00 00	fixed
1	Board area checksum	F5	checksum

Table 5-30. FRU Product Information Area

Length	Field	Value	Description
1	Product Area Format version	01	Fixed
1	Product Area length	08	Length = 56 bytes
1	Language Code (English)	19	English
1	**Manufacturer Name** type/length byte	C9	8-bit ASCII, Length= 9 Bytes
N	Manufacturer Name bytes	467265657363616c65	Freescale
1	**Product Name** type/length byte	CC	8-bit ASCII, Length= 12 Bytes
M	Product Name bytes (MPC8144AMC-S)	4D504338313434414D432D53	MPC8144AMC-S
1	**Product Part/Model Number** type/length byte	CC	8-bit ASCII, Length= 12 Bytes
O	Product Part/Model Bytes	4D504338313434414D432D53	MPC8144AMC-S
1	**Product Version** type/length byte (ASCII 12 bytes)	CD	8-bit ASCII, Length= 12 Bytes
R	Product Version Bytes	5265762042202850696C6F7429	Rev B (Pilot)
1	**Product Serial Number** type/length/bytes	C6	8-bit ASCII, Length= 6 Bytes
P	Product Serial Number (012345)	313233343536	123456

Table 5-30. FRU Product Information Area (continued)

Length	Field	Value	Description
1	**Asset Tag** type/length byte	C0	none
Q	Asset Tag	-	-
1	**FRU ID** type/length byte	C0	none
R	FRU file ID bytes	-	-
xx	Custom product info area fields	-	-
1	C1h type/length byte encoded for no more fields	C1	no more fields
Y	00h any unused fields	-	Pad with 00
1	Product Info Area Checksum	DE	checksum

Table 5-31. FRU Point to Point Connectivity Record

Length	Field	Value	Description
1	Record Type ID (C0)	C0	Fixed
1	End of List/version	02	Fixed
1	Record length	38	-
1	Record Checksum	AF	-
1	Header checksum	57	-
3	Manufacturer ID	5A3100	Fixed for PICMG at 5A3100
1	PICMG record ID (19)	19	Fixed
1	Record Format version (00)	00	Fixed
1	OEM GUID Count (1 OEM GUID record defined)	1	1 record defined
16	OEM GUID List	30303030 30303030 30303030 30303030	0000000000000000
1	Record Type	80	AMC Module
1	AMC Channel Descriptor Count	04	4 Channels
3	AMC Channel Descriptor 0	FFFFE0h	Lane 0 Port Number =0, Lanes1,2, 3 not used
3	AMC Channel Descriptor 1	FFFFE1h	Lane 0 Port Number =1, Lanes1,2, 3 not used
3	AMC Channel Descriptor 2	F398A4h	Lanes 0,1,2,3 = Port Number 4,5,6,7
3	AMC Channel Descriptor 3	F5A928h	Lanes 0,1,2,3 = Port Number 8,9,10,11
5	AMC Link Descriptor 0 Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00005100 00h 1h 05h 00h 00h 00b	AMC Link Descriptor [Breakdown below] AMC Channel ID =0 Lane 0 Bit Flag=included Link Type = AMC.2 Ethernet - Independent Match =Exact
5	AMC Link Descriptor 1 Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00005101 01h 1h 05h 00h 00h 00b	AMC Link Descriptor [Breakdown below] AMC Channel ID =1 Lane 0 Bit Flag=included Link Type = AMC.2 Ethernet - Independent Match =Exact

Table 5-31. FRU Point to Point Connectivity Record (continued)

Length	Field	Value	Description
5	AMC Link Descriptor 2 Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00006F02 02h Fh 06h 00h 00h 00b	AMC Link Descriptor [Breakdown below] AMC Channel ID =1 Lane 0,1,2,3 Bit Flag=included Link Type = AMC.4 SRIO - Independent Match =Exact
5	AMC Link Descriptor 3 Link Designator AMC Link Designator AMC Link Type AMC Link Type Extension Link grouping ID AMC Asymmetric Match	FC00006F03 03h Fh 06h 00h 00h 00b	AMC Link Descriptor [Breakdown below] AMC Channel ID =3 Lane 0,1,2,3 Bit Flag=included Link Type = AMC.4 SRIO - Independent Match =Exact

Table 5-32. FRU Module Current Requirements

Length	Field	Value	Description
1	Record Type ID (C0)	C0	Fixed
1	End of List/version (last record)	82	Last Record
1	Record length	06	Length =6 bytes
1	Record Checksum	2D	checksum
1	Header checksum	8B	checksum
3	Manufacturer ID	5A3100	Fixed for PICMG at 5A3100
1	PICMG record ID	16	Fixed
1	Record Format version (00)	00	Fixed
1	Current Draw	32	5 Amps

5.8 Boundary SCAN Testing

The card is designed to enable high percentage boundary scan test coverage. Two JTAG interfaces are used for boundary scan testing, as follows:

- The DSP JTAG header HD2 provides boundary scan coverage for the MSC8144s.
- The reset CPLD routes the TSI578, 88E1111, 88EE6185, and 88E1145 JTAGs to the AMC backplane JTAG.

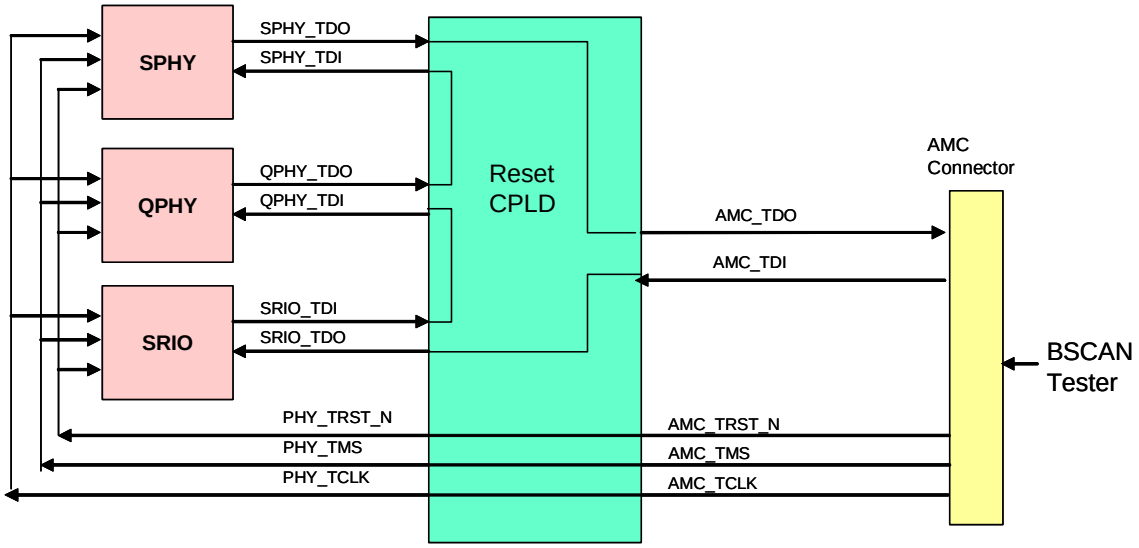


Figure 5-20. Boundary Scan Routing

5.9 Thermal Requirements

A heatsink is used to cool the MSC8144 and TSI578 devices. The heatsink definition is based on thermal simulation within an ATCA chassis with an air flow of >2 m/s. A small slip is used to ensure the heatsink makes contact with the lower profile TSI578. The AMC should be placed near the fan outlet to maximize cooling.

Chapter 6
Revision History

Table 6-1. Revision History

Revision	Date	Substantive Change(s)
0	3/2008	Initial release.
1	6/2008	Added detailed MMC information on pages 1-1, 1-3, 4-2, 4-3, and in **Section 5.7** starting on page 5-32.